

**10/03/97**

Docket: 0756-1724

Date: October 3, 1997

65705 U.S. PTO  
08/943238  
10/03/97

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

REQUEST FOR FILING

[ ] Continuation )  
 ) application under 37 CFR 1.60 (Rule 60)  
 [X] Divisional )

of pending prior application of

Applicant: Masaaki HIROKI, Akira MASE

Serial No.: 08/372,899

Group Art Unit: 2609

Filed: January 17, 1995

Examiner: L. Lao

For: ELECTRO-OPTICAL DEVICE

Honorable Assistant Commissioner for Patents

Washington, D.C. 20231

Sir:

To effect the above-requested filing today:

1. [ X ] Attached is a true copy of the prior application as filed, including  
[ X ] Specification and claims as originally filed;  
[ X ] Declaration or Oath as originally filed;  
[ X ] 45 sheets of formal drawings as originally filed
2. [ X ] The Commissioner is hereby authorized to charge fees under 37 CFR 1.16 and 1.17 (except the Issue Fee) which will be required now or hereafter, or credit any overpayment, to Deposit Account No. 19-2380. A duplicate copy of this form is attached.
3. [ ] Transfer the drawings from the prior application to this application and abandon said prior application as of the filing date accorded this application.

4. ☒ Priority is hereby claimed under Rule 55 and 35 USC 119 based on prior foreign application(s) No(s): 3-77317, 3-77320, 3-77321, 3-87776, 3-89540 filed in (country) Japan on (date) February 16, 1991 (1st three) and March 27, 1997 (4th & 5th).
- a. ☐ Certified copy(s) attached.  
☒ Certified copy(s) already filed on June 16, 1992 in prior United States Serial No. 07/837,394, filed on February 18, 1992.
5. ☒ The prior application is assigned to Semiconductor Energy Laboratory Co., Ltd.
6. ☒ The Power of Attorney in the prior application is to:
- |                         |                 |
|-------------------------|-----------------|
| Daniel W. Sixbey        | Reg. No. 20,932 |
| Stuart J. Friedman      | Reg. No. 24,312 |
| Charles M. Leedom, Jr.  | Reg. No. 26,477 |
| Gerald J. Ferguson, Jr. | Reg. No. 23,016 |
| David S. Safran         | Reg. No. 27,997 |
| Thomas W. Cole          | Reg. No. 28,290 |
- a. ☒ The Power appears in the original papers of the prior application.
- b. ☐ Since the Power does not appear in the original papers of the prior application, a copy of the Power is enclosed herewith.
7. ☐ Address all future communications to:
- SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.  
2010 Corporate Ridge, Suite 600  
McLean, Virginia 22102
8. ☒ Amend the specification by inserting before the first line the sentence --This is a Divisional application of Serial No. 08/372,899, filed January 17, 1995; which itself is a continuation of Serial No.

07/993,391, filed December 18, 1992; which is a division of  
08/837,394, filed February 18, 1992.--

9. ☒ Cancel claims 2-20.  
(DO NOT CANCEL ALL CLAIMS)

10. ☐ Status as a Small Entity is requested. Executed Small Entity  
Declaration(s)

☐ is/are attached.

☐ was/were filed in prior application on \_\_\_\_\_  
\_\_\_\_\_.

11. ☒ The filing fee is calculated below:

Claims as originally filed, less any claims above cancelled.

For:	<u>No. Filed</u>	<u>No. Extra</u>	<u>Rate</u>	<u>Fee</u>
Basic Fee				\$790.00
Total Claims	<u>1</u> - 20 =	0	x 11/22	
Indep Claims	<u>1</u> - 3 =	0	x 41/82	
<input type="checkbox"/> Multiple Dependent Claim			+ 130/260	
			TOTAL	<u>\$790.00</u>

12. ☒ Preliminary Amendment attached, to be entered at once.

Total claim fee calculated after amendment:

Total Claims	<u>20</u> - <u>20</u> ** = _____	x \$11/22****	\$
Independent Claims	<u>5</u> - <u>3</u> *** = <u>2</u>	x \$41/82****	\$164.00
	Total Amendment Fee		<u>\$164.00</u>
	Total Filing Fee		<u>\$790.00</u>
	(from paragraph 11)		
	TOTAL FEE		<u>\$954.00</u>

- Respectfully submitted,

Sixbey, Friedman, Leedom & Ferguson, P.C.  
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of )  
Masaaki HIROKI et al. )  
Based On Serial No. 08/372,899 ) Art Unit: 2609  
Which Was Filed: January 17, 1995 ) Examiner: L. Lao  
For: ELECTRO-OPTICAL DEVICE ) Date: October 3, 1997

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Please preliminarily amend the subject application as follows:

IN THE CLAIMS:

Cancel claim 1 and add new claims 21-40 as follows:

--21. A method of manufacturing a liquid crystal device comprising the steps of:

forming a gate electrode on an insulating surface of a substrate;  
forming a gate insulating film over said gate electrode;  
depositing an amorphous semiconductor film comprising silicon

on said gate insulating film;

depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing silane, phosphine and hydrogen;

patterning said n-type semiconductor layer into source and drain regions;

forming an organic leveling film over said n-type semiconductor layer after the patterning thereof; and

forming a pixel electrode over said organic leveling film.

22. A method of manufacturing a liquid crystal device according to claim 21 wherein said n-type semiconductor layer is deposited at a temperature in a range from 250°C to 320°C.

23. A method of manufacturing a liquid crystal device according to claim 21 wherein said n-type semiconductor layer is deposited by using an r.f. power of 13.56 MHz and 0.05 to 0.20 W/cm<sup>2</sup>.

24. A method of manufacturing a liquid crystal device according to claim 21 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

25. A method of manufacturing a liquid crystal device according to claim 21 wherein said gate electrode comprises aluminum.

26. A method of manufacturing a liquid crystal device according to

claim 21 wherein said gate insulating film comprises silicon oxide.

27. A method of manufacturing a liquid crystal device according to claim 21 wherein said gate insulating film comprises silicon oxide doped with fluorine.

28. A method of manufacturing a liquid crystal device according to claim 21 wherein said amorphous semiconductor film is deposited through plasma CVD.

29. A method of manufacturing a liquid crystal device according to claim 21 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

30. A method according to claim 21 wherein said silane is monosilane.

31. A method according to claim 21 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film between said source and drain regions.

32. A method of manufacturing a liquid crystal device comprising the steps of:

forming a gate electrode on an insulating surface of a substrate;  
forming a gate insulating film over said gate electrode;  
depositing an amorphous semiconductor film comprising silicon

on said gate insulating film;

depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a reactive gas including hydrogen ( $H_2$ ) gas and a monosilane-based phosphine ( $PH_3$ ) gas;

patterning said n-type semiconductor layer into source and drain regions;

forming an organic leveling film over said n-type semiconductor layer after the patterning thereof; and

forming a pixel electrode over said organic leveling film.

33. A method according to claim 32 wherein said n-type semiconductor layer has a conductivity of about  $2 \times 10^1 (\Omega cm)^{-1}$ .

34. A method according to claim 32 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film between said source and drain regions.

35. A method of manufacturing a liquid crystal device comprising the steps of:

forming a gate electrode on an insulating surface of a substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing silane, phosphine and hydrogen;

depositing a metal film on said n-type semiconductor layer;  
patterning said n-type semiconductor layer and said metal film  
into source and drain regions, and source and drain electrodes, respectively;  
forming an organic leveling film over said n-type semiconductor  
layer after the patterning thereof; and  
forming a pixel electrode over said organic leveling film,  
wherein said organic leveling film directly contacts a portion of  
said amorphous semiconductor film between said source and drain regions, and  
wherein said source and drain regions have a same pattern as said  
source and drain electrodes, respectively.

36. A method according to claim 35 wherein said silane is monosilane.

37. A method of manufacturing a liquid crystal device comprising the steps of:

forming a gate electrode on an insulating surface of a substrate;  
forming a gate insulating film over said gate electrode;  
depositing an amorphous semiconductor film comprising silicon  
on said gate insulating film;

depositing an n-type semiconductor layer on said amorphous  
semiconductor film through plasma CVD using a mixture gas containing silane,  
phosphine and hydrogen;

patterning said n-type semiconductor layer into source and drain  
regions;

forming an organic leveling film over said n-type semiconductor

layer after the patterning thereof; and

forming a pixel electrode over said organic leveling film,  
wherein said pixel electrode extends over said channel region.

38. A method according to claim 37 wherein said silane is monosilane.

39. A method according to claim 37 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film between said source and drain regions.

40. A method of manufacturing a liquid crystal device comprising the steps of:

forming a gate electrode on an insulating surface of a substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing silane, phosphine and hydrogen;

depositing a metal film on said n-type semiconductor layer;

patterning said n-type semiconductor layer and said metal film into source and drain regions, and source and drain electrodes, respectively;

forming an organic leveling film over said n-type semiconductor layer after the patterning thereof; and

forming a pixel electrode over said organic leveling film,

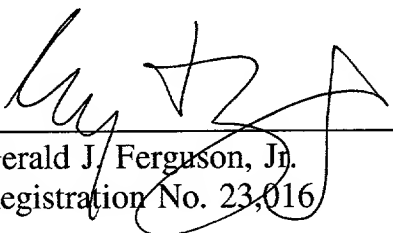
wherein inner edges of said source and drain regions are aligned with inner edges of said source and drain electrodes, respectively.--

REMARKS

New claims 21-40 have been added in this divisional application to complete the scope of applicants' protection. In this regard, it should be noted copending application Serial No. 08/776,709 is very relevant and the prior art cited in the '709 application has been cited in the Information Disclosure Statement submitted herewith.

Examination on the merits is requested.

Respectfully submitted,

  
\_\_\_\_\_  
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TITLE OF THE INVENTION

ELECTRO-OPTICAL DEVICE

BACKGROUND OF THE INVENTION

(Field of the Invention)

This invention relates to an electro-optical device and more particularly to an active-type liquid crystal display device in which clear gradated display levels can be set.

(Description of the Prior Art)

Because of the physical characteristics of the liquid crystal composition, the dielectric constant thereof differs between a direction parallel to the molecule axis and a direction perpendicular to the molecule axis, which is referred to as dielectric anisotropy, therefore the liquid crystals can easily be arranged parallel to or perpendicular to an external electric field. A liquid crystal electro-optical device utilizes this dielectric anisotropy, so that the ON/OFF display is achieved controlling the amount of light transmitted or the amount of light dispersion.

The electro-optical characteristics of a nematic liquid crystal are shown in FIG. 2. The relationship between the applied voltage and the transmissivity (amount of light transmitted) is as follows;

the applied voltage	the light transmitted
smaller $V_a$ at point A 201	0%;
$V_b$ at point B 202	about 30%;
$V_c$ at point C 203	about 80%;



larger  $V_d$  at point D 204 about 100%.

In short, if only points A and D are utilized, the two gradations, black and white, are displayed, and if the rising portion of the electro-optical characteristic curve is utilized, such as at points B and C, an intermediate gradated display is possible.

It was confirmed that  $V_a = 2.0V$ ,  $V_b = 2.18V$ ,  $V_c = 2.3V$  and  $V_d = 2.5V$ .

Conventionally, in the case of a liquid crystal electro-optical device with a gradated display utilizing a TFT, the applied gate voltage or voltage applied over the source and drains of the TFT is varied to adjust the voltage, so that an analogue gradated display is obtained.

The gradated display method with a liquid crystal electro-optical device utilizing TFTs is further described below in detail.

An n-channel thin film transistor conventionally utilized in a liquid crystal electro-optical device has the voltage-current characteristic as shown in Fig.20. In the drawing, numeral 301 designates the characteristic in case of an n-channel thin film transistor using amorphous silicon, while numeral 302 designates the characteristic in case of an n-channel thin film transistor using polycrystalline silicon.

In a conventional gradated display method, by controlling analog voltages to be applied to the gate electrode, drain currents can be controlled and accordingly the resistance value between the source and the drain can be changed. As a result, the strength of the electric fields to be applied to the liquid crystal connected thereto in series can be arbitrarily changed by the division of the resistance, whereby a gradated display is

made possible.

Also there is another method, where the gate electrode is connected to scanning signal lines and the voltage between the source and drain is changed, resulting in controlling arbitrarily the electric field value itself to be applied to the liquid crystal.

Both of the above methods are analogue gradated display methods largely relying upon the TFT characteristics. It is however difficult to form numbers of TFTs for matrix composition so as to make all of them have an uniform electric characteristic. Particularly, it is extremely difficult in the present circumstances to finely adjust the intermediate voltage necessary for a gradated display by the present techniques. As can be realized by the electro-optical characteristics of a nematic liquid crystal shown in Fig.2, a gradated display has to be carried out within 0.32V, that is, from around 2.08V, the boundary value of dark condition, to around 2.40V, the boundary value of light condition. In the case of a gradated display of 16 gradations, the control of the voltage at every 0.02V in average is required.

On the other hand, when the voltage is controlled at such as point A 201 and point D 204 shown in Fig.2 where liquid crystal is completely turned ON/OFF, the difference between voltages of 0.5V or more can be obtained, which will sufficiently ease the variation in TFT characteristics. When, using a plurality of write-in frames, for example 6 frames among 10 frames are turned ON (at 2.5V) and the remaining 4 frames are turned OFF (2.0V), the write-in voltage is 2.3V in average, so that an intermediate gradated display becomes possible.

In this case, however, the drive frequency might be

decreased to 30Hz or lower which is not discernible by the human eyes. Depending on conditions, this becomes a cause of the inferiority of a display such as flicker. Although it is proposed to raise the drive frequency to prevent the above problem, the data transfer speed of a driver IC has its limit up to about 20MHz.

#### SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a means of supplying a precise, clear level of gradated display to the liquid crystals by presenting a digital gradated display rather than a conventional analogue gradated display.

In order to obtain a good quality gradated picture, the drive frequency of the drive IC is raised and the frame frequency is not reduced substantially and the frame frequency does not fall below the visually discernable minimum frequency ( the lowest confirmed number of frames) in the method of displaying a gradated image in accordance with the present invention.

With the present invention, a gradated display is provided in an active-matrix-type liquid crystal display device, using a display drive system with the display timing related to the unit time  $t$  for writing-in a picture element and to the time  $F$  for writing-in one picture, wherein, by time-sharing the signal during a write-in of time  $t$ , without changing the time  $F$ , a gradated display corresponding to the ratio of the division is obtained since an average electric field applied to a liquid crystal at a picture element (pixel) during the time  $t$  can be controlled by controlling the ratio of the division.

For purposes of explanation, the type of 4 x 4 matrix shown

in FIG. 3 will be used.

In the case of a method for gradated display with a conventional display device, as shown in FIG. 4, the electric fields like 220 - 223 to be applied to the pixel electrodes are determined depending on the strength of the electric fields to the signal lines 210 - 213 of the data electrode direction, from which the transmittance of the liquid crystals is determined. Note reference numerals in Fig.3 corresponds to that in Fig.4.

In the present invention, this type of analogue gradation control is not used, and the signal during a write-in unit time  $t$  225 for writing in a pixel is time-shared as shown in FIG. 1, so that the gradated display can be accomplished with each of the divisions used as a minimum unit.

At this time, in the case where the electric fields 227, 229, 231 in the write-in time are changed as shown in FIG. 1, the electric fields in the non-write-in time become the average values 228, 230, 232, and a clear gradated display becomes possible.

For another explanation, the type of 2 x 2 matrix shown in Fig.10 or Fig.17 will be used.

In another method for gradated display with a conventional display device, as shown in Fig.11, a plurality of picture frames, for example, 16 frames are used, and the electric field over the picture element electrodes is determined as the average voltage for 16 frames by turning the picture elements ON and OFF, from which the transmittance of the liquid crystals is determined.

In the present invention, however, the conventional analogue gradation control or the gradated display with a plurality of frames is not used, and the signal during a write-in unit time  $t$

325 for writing in a pixel is time-shared as shown in Fig.9 and Fig.16, so that the gradated display can be accomplished with each of the divisions used as a minimum unit. In the case of the circuit shown in Fig.10, a gradated display can be obtained with the signal in Fig.9, and in the case of the circuit shown in Fig.17, a gradated display is obtained with the signal in Fig.16.

At this time, in the case where the electric fields 327, 329 in the write-in time are changed as shown in Fig.9 or Fig.16, the liquid crystals are activated by the average value of the applied voltage and a clear gradated display becomes possible.

In another method of the present invention, a digital gradated display is carried out without changing the frame frequency and with the data transfer frequency and the frequency for gradated display being independent of each other.

In the case of a liquid crystal electro-optical device having 1920 x 400 dots, for example, the data transfer on the information signal side by 8 bit parallel transfer requires the clock frequency of 5.76MHz. If the conventional method with a plurality of frames, e.g. 10 frames, is employed for this data transfer, the clock frequency as high as 57.6MHz is necessary. However, since the clock frequency for a gradated display is made independent in the present invention, a gradated display having about 166 gradations is possible with an IC driven at 8MHz in maximum. If an IC driven at 12.3MHz is used, a display having 256 gradations, which is considered necessary for a visual display, is sufficiently possible. Therefore, the gradated display in accordance with the above method is greatly advantageous over the conventional analogue gradated display and the gradated display with a plurality of frames.

Liquid crystal components which can be utilized in the

present invention are a material exhibiting ferroelectricity, a material exhibiting anti-ferroelectricity, a material consisting mainly of a nematic liquid crystal, a material consisting mainly of a cholesteric liquid crystal, a nematic liquid crystal dispersed in an organic resin, a cholesteric liquid crystal dispersed in an organic resin, and a smectic liquid crystal dispersed in an organic resin.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a graph showing an example of the drive waveforms in this invention;

Fig. 2 is a graph showing the electro-optical characteristics of the nematic liquid crystal;

Fig. 3 is an electric circuit of the NTFT matrix;

Fig. 4 is a graph showing an example of the drive waveforms in the prior art device;

Fig. 5 is a partly cut-away plan view of the device of an embodiment in the present invention;

Figs. 6 (A) to 6 (G) are cross-sectional views to show the manufacturing process of an example of this invention;

Fig. 7 shows examples of picture elements in display in this invention;

Fig. 8 shows another example of the drive waveforms in this invention.

Fig. 9 is a graph showing an example of the drive waveforms in accordance with the present invention;

Fig. 10 shows an example of the circuit configuration of a liquid crystal electro-optical device in accordance with the present invention;

Fig.11 is a graph showing another example of conventional drive waveforms;

Fig.12 shows a layout of electrodes and the like of one embodiment of the present invention;

Figs. 13(A) to 13(F) are cross-sectional view to show the formation process of a substrate of the present invention;

Fig.14 is a gradated display obtained in one embodiment of the present invention;

Fig.15 is a graph showing another example of the drive waveforms in the present invention.

Fig.16 is a graph showing another example of the drive waveform in accordance with the present invention;

Fig.17 is another example of the circuit configuration of a liquid crystal electro-optical device of the present invention;

Figs. 18 (A) to 18(F) are cross-sectional views to show the formation process of a substrate of one embodiment of the present invention;

Fig.19 is a graph showing an example of the drive waveforms in the present invention;

Fig.20 shows gate voltage-drain current characteristics in a polycrystalline silicon TFT and an amorphous silicon TFT.

Fig.21 is another example of the circuit configuration of a liquid crystal electro-optical device of the present invention;

Figs.22(A) to 22(I) are cross-sectional views to show the manufacturing process of another example of the present invention;

Figs.23(A) to 23(E) are cross-sectional views to show the formation process of a substrate of the present invention;

Fig.24 shows a schematical configuration of an electro-optical device of one embodiment of the present invention;

Fig.25 shows the peripheral circuitry of a liquid crystal electro-optical device of the present invention;

Figs.26(A) to 26(E) are cross-sectional views to show the manufacturing process of a liquid crystal device of one embodiment of the present invention;

Fig.27 shows an assembly of a projection type image display of one embodiment of the present invention;

Figs.28(A) to 28(G) are cross-sectional views to show the manufacturing process of a liquid crystal display device of one embodiment of the present invention;

Fig.29 shows a schematic configuration of a liquid crystal electro-optical device of one embodiment of the present invention;

Fig.30 shows a schematic configuration of a reflection type liquid crystal dispersion display device of one embodiment of the present invention;

Fig.31 is an example of the circuit configuration of a liquid crystal display device of the present invention;

Fig.32 is a layout of electrodes and the like of another embodiment of the present invention;

Figs.33(A) to 33(H) are cross-sectional views to show the manufacturing process for a liquid crystal panel of one embodiment of the present invention;

Fig.34 shows the peripheral circuitry of a liquid crystal electro-optical device of the present invention;

Figs.35(A) to 35(D) are graphs showing input signal waveforms inputted to and output signal waveforms outputted from the C/TFT obtained in one embodiment of the present invention;

Figs.36(A) to 36(G) are cross-sectional views to show the manufacturing process for a liquid crystal display device of one



embodiment of the present invention;

Fig.37 is a layout of electrodes and the like of another embodiment of the present invention;

Fig.38 is a layout of electrodes and the like of still another embodiment of the present invention;

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

##### [Embodiment 1]

In this embodiment, a liquid crystal display device with the circuit configuration shown in FIG. 17, that is, a buffer type circuit configuration, is used.

FIG. 38 shows the layout of the actual electrodes and the like corresponding to the circuit configuration of FIG. 17.

In order to simplify the explanation, the parts corresponding to a 2 x 2 matrix only are described.

Also, the actual driving signal waveform is shown in FIG. 16. For simplicity, the explanation of the signal waveform is also given for the case of 2 x 2 matrix configuration.

The manufacturing process for forming the substrate for the liquid crystal display device used in an embodiment of the present invention is shown in FIG. 18.

In Fig. 18(A), a silicon oxide film for a blocking layer 951 having a thickness of 1000 to 3000 angstroms was formed on a glass substrate 950, using a magnetron RF (high frequency) sputtering method. The glass substrate 950 was made of inexpensive glass capable of withstanding heat treatment up to 700 °C e.g. of 600 °C.

The process conditions were as follows:

atmosphere: 100% oxygen

film forming temperature: 150 °C

output: 400 to 800 W

pressure: 0.5 Pa

The film forming, using either quartz or single-crystal silicon for a target had a speed of 30 to 100 Angstroms/minute.

On top of this construction, an amorphous silicon film was formed using an LPCVD (low pressure chemical vapor deposition) method, sputtering method, or a plasma CVD method.

If using the LPCVD method to form the silicon film, disilane ( $\text{Si}_2\text{H}_6$ ) or trisilane ( $\text{Si}_3\text{H}_8$ ) was supplied to the CVD apparatus at a temperature 100 to 200 °C less than the crystallization temperature, that is, 450 to 550 °C, for example at 530 °C. The pressure inside the reaction furnace was 30 to 300 Pa. The film forming speed was 50 to 250 Å/minute.

In order to control the threshold voltage ( $V_{th}$ ) of both the NTFT and PTFT at a substantially same level, boron with a concentration of  $1 \times 10^{15}$  to  $5 \times 10^{18} \text{ cm}^{-3}$  can be added using diborane.

In the case of using a sputtering method, the conditions were as follows;

back pressure before sputtering: up to  $1 \times 10^{-5}$  Pa

target: a single crystal silicon

atmosphere: argon with hydrogen 20 to 80% by volume

e.g. 20 volume % Ar and 80 volume %  $\text{H}_2$

the film forming temperature: 150 °C

frequency: 13.56 MHz

sputter output: 400 to 800W

pressure: 0.5 Pa

In the case of forming a silicon film using the plasma CVD method, the temperature was 300 °C for example, and monosilane

(SiH<sub>4</sub>) or disilane (Si<sub>2</sub>H<sub>6</sub>) was used as the reactive gas, which were input into a PCVD apparatus and 13.56 MHz high frequency electric power was applied for film forming.

In this method, it is preferable that the oxygen concentration of the film formed is  $5 \times 10^{21} \text{ cm}^{-3}$  or less. If the oxygen concentration is higher than this range, crystallization becomes difficult and the heat annealing temperature must be high or the annealing time long. On the other hand, if the concentration is too low, the current leak in the OFF state increases because of the back light. For this reason the concentration is held in the range from  $4 \times 10^{19}$  to  $4 \times 10^{21} \text{ cm}^{-3}$ . Silicon concentration was assumed to be  $4 \times 10^{22} \text{ cm}^{-3}$  and hydrogen concentration was  $4 \times 10^{20} \text{ cm}^{-3}$ , which is equal to one atomic % of the silicon concentration.

Also, to promote further crystallization at the source and drain, the oxygen concentration is adjusted to  $7 \times 10^{19} \text{ cm}^{-3}$  or less, or, preferably,  $1 \times 10^{19} \text{ cm}^{-3}$  or less, and oxygen may be added by ion implantation to a concentration range of  $5 \times 10^{20}$  to  $5 \times 10^{21} \text{ cm}^{-3}$ , only to the channel forming regions of the TFTs which form the pixels. On the other hand, it is effective for a high frequency operation to reduce the amount of oxygen contained in the TFT provided in the peripheral circuits which no light reaches, so as to make the carrier mobility greater.

After the amorphous silicon film was formed to a thickness of 500 to 5000 Å, for example 1500 Å by means of the foregoing process, an intermediate heat treatment was performed at 450 to 700 °C for 12 to 70 hours in an oxygen-free atmosphere, for example, in a hydrogen atmosphere at 600 °C.

Because an amorphous silicon oxide film was formed on the surface of the substrate beneath the silicon film, no specific

nucleus existed in this heat treatment so the whole amorphous silicon film was uniformly heat annealed. Specifically, the amorphous structure was kept in film forming and hydrogen was merely mixed in.

It was supposed that when annealing the silicon film, crystallization was inclined to take place in a highly ordered state from the amorphous structure, so that a crystal state was partly produced. Particularly, in the regions where a relatively highly ordered state was produced just after film forming of silicon, the tendency of crystallization to a crystal state was strong. A junction, however, took place due to the silicon between these regions, so that the silicon attracted each other.

According to laser Raman spectrometry measurement of the annealed silicon film, it was observed that a peak thereof was shifted from  $522\text{ cm}^{-1}$  of the single crystal silicon to a lower frequency side. The apparent grain diameter, when calculated using the half-value width, was 50 to 500 Å, like a micro crystal. Actually, there were many of these highly crystallized regions that made up clusters. Each cluster was joined to the other by a silicon junction (anchoring) forming a semi-amorphous film.

Consequently, it was believed that the film could be said to have substantially no grain boundary (GB). The carriers could easily travel between the clusters through the anchored areas, so the mobility of the carriers was higher than that of the polycrystalline silicon having clear grain boundaries (GB).

The Hall mobility obtained was ( $\mu_h$ ) = 10 to 200  $\text{cm}^2/\text{Vsec}$ , and the electron mobility obtained was ( $\mu_e$ ) = 15 to 300  $\text{cm}^2/\text{Vsec}$ .

When the film is polycrystallized at a higher temperature of 900 to 1200 °C and not an intermediate temperature above,

segregation of impurities occurs due to the growth of solid phase from nucleus in the film, and there are a lot of impurities such as oxygen, carbon, nitrogen in GB. Therefore, the mobility is large in the crystal, but the movement of carriers is prohibited by the barrier at GB. Consequently, it is actually impossible to obtain the mobility of  $10 \text{ cm}^2/\text{Vsec.}$  or more.

This is a reason why a silicon semiconductor with a semiamorphous or semicrystalline structure is used in this embodiment. Of course, other crystalline semiconductor materials having a high mobility can be used in the present invention.

FIG. 18(A) shows the silicon film which was photoetched using a first photomask (91), with the NTFT region 913 (20  $\mu\text{m}$  in channel width) prepared at the left side of the drawing and the PTFT region 922 at the right side.

A silicon oxide film was then formed as a gate insulation film in the thickness range of 500 to 2000  $\text{\AA}$ , for example, 1000  $\text{\AA}$ . This is prepared under the same conditions as the silicone oxide film formed as a blocking layer. A small amount of fluorine may be added to this film for fixation of the sodium ion during film forming.

When this operation was completed, a silicon film was provided containing a  $1 \text{ to } 5 \times 10^{21} \text{ cm}^{-3}$  concentration of phosphorus. Molybdenum (Mo), tungsten (W),  $\text{MoSi}_2$  or  $\text{WSi}_2$  film may be optionally formed on this silicon film to form a multilayer film. The silicon film (or multilayer film) was patterned with a second photomask (92) to obtain the configuration shown in FIG. 18(B). An NTFT gate electrode 909 and a PTFT gate electrode 921 were then formed. For example, as a gate electrode, a phosphorus-doped silicon 0.2  $\mu\text{m}$  thick was formed and a molybdenum layer 0.3  $\mu\text{m}$  thick was formed thereon with a channel length of 10  $\mu\text{m}$ .

As shown in FIG. 18(C), a photoresist 957 was formed using a photomask (93), and boron was added using the ion implantation method at a dosage of  $1 \text{ to } 5 \times 10^{15} \text{ cm}^{-2}$  for the PTFT source 918 and drain 920. Next, as illustrated in FIG. 18(D), a photoresist 961 was formed using a photomask (94). Phosphorous was added using the ion implantation method at a dosage of  $1 \text{ to } 5 \times 10^{15} \text{ cm}^{-2}$  for an NTFT source 910 and drain 912.

Also, in the case where aluminum is used as the gate electrode material, after patterning with the second photomask (92), it is possible to form the source and drain contact holes at positions closer to the gate by anodic oxidation of this surface of the patterned aluminum gate electrode so that self-aligning construction can be applied. Therefore, the TFT characteristics can be further increased by improving the mobility and decreasing the threshold voltage.

The doping above is made through a gate insulation film 954. However, in FIG. 18(B), using the gate electrodes 921, 909 as a mask the silicone oxide on the silicone film may be removed, followed by the addition of the boron and phosphorous directly into the silicon film using the ion implantation method.

Next, annealing was again conducted for 10 to 50 hours at  $600^\circ\text{C}$ . The impurities of the NTFT source 910 and drain 912, and the PTFT source 918, and drain 920, were activated to form  $\text{P}^+$  and  $\text{N}^+$  regions. The channels 919 and 911 below the gate electrodes 921 and 909 were made of a semi-amorphous semiconductor.

The entire manufacturing process for the C/TFT can thus be done without having to apply a temperature above  $700^\circ\text{C}$  in the self-aligning system. This makes it possible to use other materials other than expensive quartz as the substrate material. Accordingly, this embodiment of the invention is very suitable

for a liquid crystal display having a large picture element.

The heat anneal process, shown in Fig. 18(A) and Fig. 18(D), was performed twice. However, the anneal process of Fig. 18(A) can be omitted, depending on the desired characteristics, and followed up with the heat anneal process of Fig. 18(D), shortening the manufacturing time. Also, in Fig. 18(E), the interlayer insulation layer 965 was made of silicon oxide film using the sputtering method mentioned above.

This silicon oxide film can, however, also be formed using the LPCVD method or photo CVD method or normal pressure CVD method.

The thickness of the insulation layer was e.g. 0.2 to 0.6  $\mu\text{m}$ .

Next, using photo mask (95), a window 966 for the electrodes was formed. Then, a layer of aluminum was formed over the entire structure using the sputtering method, and leads 971 and 972 and contacts 967, 968 were made using photo mask (96).

An organic resin film 969 for surface-flattening, e.g. a transparent polyimide resin film was formed, and electrode openings were provided using photomask (97).

Two TFTS were formed in a complementary structure in a picture element of the liquid crystal display device as shown in FIG. 18(F), in which the output terminal of the TFTS was each connected to the (transparent) electrode of the picture element of the liquid crystal display device, forming the ITO (Indium Tin Oxide) by sputtering.

The electrode 917 was completed by etching through the photomask (98).

This ITO film was formed in the range from room temperature to 150 °C and finished by annealing at 200 °C to 400 °C in oxygen

or atmosphere. The NTFT 913, the PTFT 922 and the transparent electrode 917 were thus prepared on a single glass substrate 950.

The electrical characteristics of the TFT obtained thus are as follows:

mobility in the PTFT:  $20 \text{ cm}^2/\text{Vs}$

$V_{th}$  in the PTFT:  $-5.9 \text{ V}$

mobility in NTFT:  $40 \text{ cm}^2/\text{Vs}$

$V_{th}$  in NTFT:  $5.0 \text{ V}$

Another glass substrate provided with a transparent electrode over the entire surface thereof and the substrate fabricated according to the above-described method were combined to form a liquid crystal cell. A TN liquid crystal material was injected into the liquid crystal cell. FIG. 38 illustrates the positioning of the electrodes and the like for the liquid crystal display device according to this embodiment.

An NTFT 913 is provided at the intersection of a first signal line 905 and a third signal line 903, and, in the same manner, an NTFT for another picture element is provided at the intersection of the first signal line 905 and a third signal line 904. A PTFT is provided at the intersection of a second signal line 908 and the third signal line 903. Also, an NTFT for another picture element is provided at the intersection of another, adjacent first signal line 906 and the third signal line 903, while in the same manner an NTFT is provided at the intersection of the first signal line 906 and the third signal line 904.

The NTFT 913 is connected to the first signal line 905 through a contact on the input terminal on the drain 910, and the gate 909 is connected to a signal line 903 which is formed of multilayer wiring. The output terminal of the source 912 is



connected to a picture element electrode 917 through a contact.

The PTFT 922 is connected to the second signal line 908 through a contact on the input terminal on the drain 920, wherein the gate 921 is connected to the signal line 903, and the output terminal of the source 918 is connected to the picture element electrode 917 through a contact in the same way as in the NTFT.

Adjacently, another C/TFT which is connected to the same signal line 903 is provided and the PTFT 922 of said another C/TFT is connected to a second signal line 907, and the NTFT 913 of said another C/TFT is connected to the first signal line 906.

One pixel comprising a picture element 923 formed from a transparent conducting film and a C/TFT is interposed between this pair of signal lines 905 and 908. By repeating this type of configuration laterally and vertically, the 2 x 2 matrix can be expanded to form a large picture element liquid crystal display device of 640 x 480 or 1280 x 960 matrixes.

A special feature of this device is that the picture element electrode 917 is set at three values of the liquid crystal potential  $V_{LC}$  by providing a complementary configuration of two TFTs for one picture element.

Next, in order to form a second substrate, an ITO film (Indium Tin Oxide) was formed by sputtering on a substrate which was formed by laminating a silicon oxide film to a thickness of 2000 Å on glass plate by the sputtering process. This ITO film was formed in the range from room temperature to 150 °C and finished by annealing at 200 °C to 400 °C in oxygen or atmosphere.

A polyimide precursor member was printed on the above-mentioned substrate using the offset method and fired for one hour at 350 °C in an oxygen-free atmosphere (for example, in a nitrogen atmosphere). The polyimide surface was then reformed

using a commonly known rubbing method, so that a means for orienting the liquid crystal molecules in a uniform direction in at least the initial stage was provided, whereby the second substrate was completed.

Then, the liquid crystal composition having ferroelectricity was interposed between the first and second substrates, and the assembly was sealed around the periphery using an epoxy-type adhesive. A drive IC of a TAB form was connected to a lead on the substrate and a polarizing plate was affixed to the outside to obtain a light-transmission type of liquid crystal display device.

FIG. 14 shows the display for the A, E, and C picture elements when the drive waveform shown in FIG. 16 is applied. In Fig.14, darkness is expressed by a dot. A clear gradated display is obtained, as shown in Fig.14.

#### [Embodiment 2]

In this embodiment, a first substrate and a second substrate were obtained using the same process as for the Embodiment 1. However, no polyimide film for alignment was formed on the second substrate. Since this device was made for use in a video camera viewfinder, the pitch of the picture element was 60  $\mu\text{m}$ , and a matrix 200 high x 300 wide was formed.

In this embodiment, a nematic liquid crystal composition was dispersed throughout an acrylic organic resin to form a dispersed-type liquid crystal display device. 62 wt% of the nematic liquid crystals was dispersed throughout an acrylic resin denatured with an ultraviolet-curable epoxy. This material was interposed between the first and second substrates, then cured by

the application of a light beam from a UV light source with a 1000 mW output for 20 sec.

This display device was time-shared into 16 to provide a gradated display, and each color had 16 gradations, to give a liquid crystal display device which can display a total of 4096 colors. The drive wave form at that time is shown in FIG. 19.

In summary, a plurality of write-in entries (display frames) is provided in conventional gradated display methods. For example, 16 frames are utilized to provide a method for presenting a gradated display by a combination of their ON/OFF states. If, in a total 16 frames, eight frames are ON and the remaining eight frames are OFF, a gradated display results at a 50% transmission, which is the average transmittance in this case.

If, however, four frames are ON and the remaining 12 frames are OFF, the average transmittance becomes 25% and a gradated display occurs at this transmission.

When this conventional method is used there is a strong possibility of the number of frames less than the lowest confirmed number of frames, 30 frames, which are the minimum number of frames that can be discerned by the human eye. This is the main cause of a drop in the quality of the display.

In this embodiment, where the frequency of the driver is increased for providing a gradated display of the present invention, a gradated display becomes possible preventing the actual frame frequency from decreasing. Therefore, the frequency never becomes lower than a visually confirmed frequency, so that a drop in display quality does not occur, and a high quality picture can be provided.

By using the same type of process and drive method it is possible to provide a word processor screen, a computer screen,

or a device for projecting a visual image display.

#### [Embodiment 3]

The liquid crystal electro-optical device utilized in this embodiment has the circuit configuration shown in Fig.10, namely, the circuit configuration of inverter type. FIG. 12 shows the layout of the actual electrodes and the like corresponding to the circuit configuration of FIG. 10. In order to simplify the explanation, the parts corresponding to a 2 x 2 matrix only are described. Also, the actual driving signal waveform is shown in Fig.9.

The process for forming a substrate for the liquid crystal electro-optical device utilized in this embodiment is shown in Figs.13(A) to (F). In accordance with the process shown in Figs. 13(A) to (F), the substrate shown in Fig.13(F) was formed in the same manner as in Embodiment 1. The substrate had the same structure as that in Embodiment 1 except that the location of a PTFT and an NTFT thereof was opposite to that of Embodiment 1, as shown in Figs.10 and 13. With thus obtained substrate, a light-transmission type liquid crystal electro-optical device was completed as in Embodiment 1.

#### [Embodiment 4]

In this embodiment, a first substrate and a second substrate were obtained using the same process as for Embodiment 3. However, an orientation film made of polyimide was not formed on the second substrate. With these first and second substrates, a

liquid crystal electro-optical device for use in a video camera viewfinder was formed at a pitch of a picture element of  $60\mu\text{m}$ , and a matrix 200 high x 300 wide in the same way as in Embodiment 2.

In this embodiment, where the frequency of the driver is increased for providing a gradated display of the present invention, a gradated display becomes possible preventing the actual frame frequency from decreasing. Therefore, the frequency never becomes lower than a visually confirmed frequency, so that a drop in display quality does not occur, and a high quality picture can be provided.

By using the same type of process and drive method it is possible to provide a word processor screen, a computer screen, or a device for projecting a visual image display.

In the drive method of the present invention shown in Fig.15 where the unit time  $t$  225 for writing-in a picture element is divided into 16 minimum units (a period of each minimum unit 227 is  $t/16$ ), each color is displayed with 16 gradations, so that a display with 4096 colors is possible in total.

#### [Embodiment 5]

In this embodiment, a liquid crystal display device with the circuit configuration shown in FIG. 3 is used.

FIG. 5 shows the layout of the actual electrodes and the like corresponding to the circuit configuration of FIG. 3.

In order to simplify the explanation, the parts corresponding to a 4 x 4 matrix (2 x 2 matrix) only are described.

Also, the actual driving signal waveform is shown in FIG. 1. For simplicity, the explanation of the signal waveform is also

given for the case of 4 x 4 matrix configuration.

The manufacturing process for the liquid crystal display device used in this embodiment is shown in FIG. 6.

In Fig. 6(A), a silicon oxide film for a blocking layer 51 having a thickness of 1000 to 3000 angstroms was formed on a glass substrate 50, using a magnetron RF (high frequency) sputtering method. The glass substrate 50 utilized was the one which was not expensive unlike quartz glass and was resistant to heat treatment up to 700 °C e.g. of 600 °C. The conditions for the process are as follows:

Atmosphere: 100% oxygen

Film Formation Temperature: 150°C

Output Power: 400 - 800W

Pressure: 0.5Pa

The film formation, using either quartz or single-crystal silicon for a target, had a speed of 30 to 100 Å/min.

On the top surface thereof, a silicon film in an amorphous state having a thickness of 500 to 5000Å, e.g. 1500Å, was formed as in Embodiment 1. In the case of using low pressure CVD method to form the amorphous silicon film as in Embodiment 1, boron may be added at a concentration of  $1 \times 10^{15}$  to  $1 \times 10^{18}$  cm<sup>-3</sup> by the use of diborane during the film formation, in order to control the threshold voltage (V<sub>th</sub>) of the NTFT.

Then, in the same manner as in Embodiment 1, the silicon film in an amorphous state was heat-annealed at an intermediate temperature of 450 to 700°C for 12 to 70 hours under a non-oxide atmosphere. Then, an NTFT region 13 was obtained from the silicon film by the use of a first photomask (1).

A silicon oxide film was then formed as a gate insulating film 54 in the thickness range of 500 to 2000Å, for example,

1000Å. This is prepared under the same conditions as the silicone oxide film formed as a blocking layer. A small amount of fluorine may be added to the film for fixation of the sodium ion during the film formation.

When this operation was completed, a silicon film containing a  $1 \text{ to } 5 \times 10^{21} \text{ cm}^{-3}$  concentration of phosphorus, or a multilayered film comprising the silicon film laminated thereon with molybdenum (Mo), tungsten (W),  $\text{MoSi}_2$  or  $\text{WSi}_2$  film was formed, which was then patterned with a second photomask (2) to obtain the configuration shown in FIG. 6(B). Phosphorus was added by ion implantation method at a dosage of  $1 \text{ to } 5 \times 10^{15} \text{ cm}^{-2}$  for a NTFT source 20 and drain 18, using the gate electrode 9 as a mask.

Also, in the case where aluminum is used as the gate electrode material, after patterning with the second photomask (2), it is possible to form the source and drain contact holes at positions closer to the gate by anodic oxidation of this surface of the patterned aluminum gate electrode so that self-aligning construction can be applied. Therefore, the TFT characteristics can be further increased by improving the mobility and decreasing the threshold voltage.

The above process is carried out through the gate insulating film 54. However, in FIG. 6(B), it is possible to remove the silicon oxide formed on the silicon film using the gate electrode 9 as a mask and then add the phosphorus directly into the silicon film using the ion implantation method.

Next, annealing was again conducted for 10 to 50 hours at  $600^\circ\text{C}$ . The impurities were activated whereby the source 20 and drain 18 of the NTFT were made  $\text{N}^+$  regions. A channel forming region 21 of semi-amorphous semiconductor was formed below the

gate electrode 9.

The entire manufacturing process for the NTFT can thus be done without having to apply a temperature above 700°C in spite of the self-aligning system. This makes it possible to use materials other than expensive ones such as quartz for the substrate material. Accordingly, this embodiment of the invention is very suitable for a liquid crystal display having a large number of pixels.

The heat anneal process was carried out twice as shown in Figs. 6(A) and (C). However, the anneal process of Fig. 6(A) may be omitted, depending on the desired characteristics, and followed up with the heat anneal process of Fig. 6(C), shortening the manufacturing time. Also, in Fig. 6(D), the interlayer insulating layer 65 was made of silicon oxide film using the sputtering method mentioned above.

This silicon oxide film can, however, also be formed using the LPCVD method or photo CVD method or normal pressure CVD method. The thickness of the film was e.g. 0.2 to 0.6μm.

Next, using photo mask (3), an opening 66 for the electrodes was formed. Then, a layer of aluminum was formed on the entire surface by sputtering, and leads 71 and 72 and contacts 67, 68 were formed by using photo mask (4).

An organic resin film 69 for surface-flattening, e.g. a transparent polyimide resin film was formed, and openings for electrodes were provided using a photomask (5).

The TFT was thus formed as shown in FIG. 6(F), and further an ITO (Indium Tin Oxide) film was formed by sputtering in order that the output terminal of the TFT was connected to a transparent electrode of the picture element of the liquid crystal display device by the ITO.



The electrode was completed by etching the ITO film through a photomask ⑥, whereby a pixel electrode 17 and a contact 73 of the pixel electrode with the drain electrode were completed. This ITO film was formed in the range from room temperature to 150°C and annealed at 200° to 400°C in oxygen or atmosphere.

The NTFT 13 and the transparent pixel electrode 17 were thus prepared on an identical glass substrate 50.

The electrical characteristics of the TFT thus formed are as follows:

mobility: 40 cm<sup>2</sup>/Vs

V<sub>th</sub>: 5.0 V.

The first substrate was thus completed.

Then, a second substrate was manufactured in the same manner as the second substrate of Embodiment 1.

Then, the liquid crystal composition exhibiting ferroelectricity was interposed between the first and second substrates, and the assembly was sealed around the periphery using an epoxy-type adhesive. A drive IC of a TAB form was connected to a lead on the substrate and a polarizing plate was affixed to the outside to obtain a light-transmission type of liquid crystal display device.

FIG. 7 shows the display for the A, F, and I picture elements when the drive waveform shown in FIG. 1 is applied. This figure shows that a clear gradated display is obtained.

#### [Embodiment 6]

In this embodiment, a first substrate and a second substrate were obtained using the same process as for Embodiment 5. However, an orientation film made of polyimide was not formed on

the second substrate. With these first and second substrates, a liquid crystal electro-optical device for use in a video camera viewfinder was formed at a pitch of a picture element of  $60\mu\text{m}$  and a matrix 200 high x 300 wide in the same way as in Embodiment 2.

In the drive method of the present invention shown in Fig.8 where the unit time  $t$  for writing-in a picture element is divided into 16 minimum units ( a period of each minimum unit is  $t/16$ ), each color is displayed with 16 gradations, so that a display with 4096 colors is possible in total.

In this embodiment, where the frequency of the driver is increased for providing a gradated display of the present invention, a gradated display becomes possible preventing the actual frame frequency from decreasing. Therefore, the frequency never becomes lower than a visually confirmed frequency, so that a drop in display quality does not occur, and a high quality picture can be provided.

It is effective to improve the ability of gradated display over the conventional one by conducting the above-mentioned conventional method for gradated display together with the method for gradated display in accordance with the present invention. The method of the present invention is to control the average voltage applied to a liquid crystal pixel, where complete response of liquid crystal is not required.

Conventionally, it was difficult to directly apply the voltages  $V_b$  and  $V_c$  shown in Fig.2 to pixels. However, by changing the average of the voltage applied to pixel electrodes, an effect can be obtained as if the voltages  $V_b$  and  $V_c$  were directly applied to pixels.

In other words, the present invention is to provide a method for controlling liquid crystal which responds incompletely.

Although only N-channel field effect transistors are utilized in this embodiment, P-channel field effect transistors may be utilized instead.

[Embodiment 7]

In this embodiment, a liquid crystal electro-optical device (image display device) with the circuit configuration shown in Fig.21 is utilized as a television to be hanged on the wall. The TFTs utilized therein are made of polycrystal silicon subjected to laser annealing and are of stagger type.

Referring to Fig.21, a reference numeral 700 designates a gate electrode, 701 a source, 702 a drain, 703 a NMOSTFT, and 704 a pixel electrode.

The layout of the actual electrodes and the like corresponding to the circuit configuration in Fig.21 is shown in Fig.37. For simplifying the explanation, the parts corresponding to a 2 x 2 (or less) matrix only are described. Also, the reference numerals are made so as to correspond to those in Fig.21.

The reference numeral 705 designates a lead contact and 706 a pixel contact.

Further, the actual driving signal waveform is shown in Fig.1. For simplicity, the explanation of the signal waveform is also given for the case of 4 x 4 matrix configuration.

The manufacturing process for the liquid crystal display device used in this embodiment is shown in FIG.22.

In Fig.22(A), a silicon oxide film for a blocking layer 801 having a thickness of 1000 to 3000 angstroms was formed on a glass substrate 800, using a magnetron RF (high frequency) sput-

tering method. The glass substrate 800 utilized was the one which was not expensive unlike quartz glass and was resistant to heat treatment up to 700 °C e.g. of 600 °C. The conditions for the process are as follows:

Atmosphere: 100% oxygen

Film Formation Temperature: 150°C

Output Power: 400 - 800W

Pressure: 0.5Pa

The film formation, using either quartz or single-crystal silicon for a target, had a speed of 30 to 100 Å/min.

On this silicon oxide film, a silicon film in an amorphous state was formed. In the case of using plasma CVD method to form this amorphous silicon film, the film formation temperature was from 250° to 350°C, e.g. 320°C in this embodiment, and monosilane ( $\text{SiH}_4$ ) was utilized. However, disilane ( $\text{Si}_2\text{H}_6$ ) or trisilane ( $\text{Si}_3\text{H}_8$ ) may be utilized instead of monosilane. The gas was inputted to a PCVD apparatus maintained at a pressure of 3 Pa and a high frequency electric power was applied thereto at a frequency of 13.56 MHz, whereby the silicon film was deposited. A high frequency electric power of 0.02 to  $0.10\text{W}/\text{cm}^2$  was appropriate in this case, and in this embodiment a high frequency electric power of  $0.055\text{W}/\text{cm}^2$  was applied. The flux of the monosilane was at 20SCCM and the film formation rate under this condition was about 120Å/min.

Boron may be added at a concentration of  $1 \times 10^{15}$  to  $1 \times 10^{18}\text{cm}^{-3}$  by using diborane during the film formation, in order to control the threshold voltage ( $V_{th}$ ) of the NTFT.

Not only this plasma CVD method but also sputtering method and low pressure CVD method can be utilized for forming the silicon film to be a channel region in a TFT.

In the case of using a sputtering method, the conditions were as follows:

back pressure before sputtering: up to  $1 \times 10^{-5}$  Pa  
target: a single crystal silicon  
atmosphere: argon with hydrogen 20 to 80% by volume  
e.g. 20 volume % Ar and 80 volume %  $H_2$   
the film forming temperature: 150 C  
frequency: 13.56 MHz  
sputter output: 400 to 800W  
pressure: 0.5 Pa

If using the LPCVD method to form the silicon film, disilane ( $Si_2H_6$ ) or trisilane ( $Si_3H_8$ ) was supplied to the CVD apparatus at a temperature 100 to 200 °C less than the crystallization temperature, that is, 450 to 550 °C, for example at 530 °C. The pressure inside the reaction furnace was 30 to 300 Pa. The film forming speed was 50 to 250 Å/minute.

With respect to the film formed by these methods, it is preferable that the oxygen concentration is  $5 \times 10^{21} \text{ cm}^{-3}$  or less. In order to promote crystallization of the film, it is desirable that the oxygen concentration is  $7 \times 10^{19} \text{ cm}^{-3}$  or less, preferably  $1 \times 10^{19} \text{ cm}^{-3}$  or less. However, if the concentration is too low, the current leak in the OFF state increases because of the back light. If the oxygen concentration is too high, crystallization becomes difficult and the laser annealing temperature must be increased or the annealing time lengthened. Silicon concentration was assumed to be  $4 \times 10^{22} \text{ cm}^{-3}$  and hydrogen concentration was  $4 \times 10^{20} \text{ cm}^{-3}$  which is equal to one atomic % of the silicon concentration.

Also, to promote further crystallization at the source and drain, the oxygen concentration is adjusted to  $7 \times 10^{19} \text{ cm}^{-3}$  or

less, or, preferably,  $1 \times 10^{19} \text{ cm}^{-3}$  or less, and oxygen may be added by ion implantation to a concentration range of  $5 \times 10^{20}$  to  $5 \times 10^{21} \text{ cm}^{-3}$ , only to the channel forming regions of the TFTs which form the pixels.

By the above method, the silicon film 802 in an amorphous state was formed to be 500 to 5000Å in thickness, e.g. 1000Å in this embodiment.

Then, photoresist 803 was formed in a pattern having openings therein on source and drain regions as shown in Fig.22(B) by the use of a mask (1). On this structure, a silicon film 804 to be an n-type activation layer was formed by plasma CVD. The film formation temperature was 250° to 350°C, specifically 320°C in this embodiment. Monosilane ( $\text{SiH}_4$ ) and phosphine ( $\text{PH}_3$ ) of monosilane base at a concentration of 3% were utilized. They were introduced into a PCVD apparatus maintained at a pressure of 5 Pa and an electric power at a high frequency of 13.56MHz was inputted thereto, whereby the silicon film 804 was deposited. The high frequency electric power of 0.05 to  $0.20\text{W}/\text{cm}^2$  was appropriate in this case, and in this embodiment an electric power of  $0.120\text{W}/\text{cm}^2$  was inputted.

The n-type silicon film formed by the above method had a specific electric conductivity of about  $2 \times 10^{-1} [\Omega \text{cm}^{-1}]$ . The thickness thereof was 50Å. Then, source and drain regions 805 and 806 were formed by lift-off method. After that, an island region 807 for an N-channel thin film transistor was formed using a mask 82.

Subsequently, laser annealing to the source, drain, channel regions and laser doping to the activation layer were carried out simultaneously by the use of XeCl excimer laser. The threshold energy of this laser at this moment was  $130\text{mJ}/\text{cm}^2$ . On the other

hand, in order to melt the whole film thickness, the energy of  $220\text{mJ}/\text{cm}^2$  was necessary. However, if a laser having an energy more than  $220\text{mJ}/\text{cm}^2$  was irradiated from the beginning, hydrogen contained in the film would be discharged rapidly, resulting in the destroy of the film. For this reason, it is necessary to firstly discharge the hydrogen at a low energy and then melt the film. In this embodiment, a laser at  $150\text{mJ}/\text{cm}^2$  was irradiated to discharge hydrogen and then a laser at  $230\text{mJ}/\text{cm}^2$  was irradiated to crystallize the film.

It was supposed that when annealing the silicon film, crystallization was inclined to take place in a highly ordered state from the amorphous structure, so that a crystal state was partly produced. Particularly, in the regions where a relatively highly ordered state was produced just after film forming of silicon, the tendency of crystallization to a crystal state was strong. A junction, however, took place due to the silicon between these regions, so that the silicon attracted each other.

According to laser Raman spectrometry measurement of the annealed silicon film, it was observed that a peak thereof was shifted from  $522\text{ cm}^{-1}$  of the single crystal silicon to a lower frequency side. The apparent grain diameter, when calculated using the half-value width, was 50 to 500 Å. Actually, there were many of these highly crystallized regions that made up clusters. Each cluster was joined to the other by a silicon junction (anchoring) forming a film.

Consequently, it was believed that the film could be said to have substantially no grain boundary (GB). The carriers could easily travel between the clusters through the anchored areas, so the mobility of the carriers was higher than that of the polycrystalline silicon having clear grain boundaries (GB). The

electron mobility ( $\mu_e$ ) obtained was 15 to 300  $\text{cm}^2/\text{Vsec}$ .

A silicon oxide film 808 was then formed as a gate insulating film in the thickness range of 500 to 2000Å, for example, 1000Å. This is prepared under the same conditions as the silicon oxide film formed as a blocking layer. A small amount of fluorine may be added to this film for fixation of the sodium ion during film formation.

When this operation was completed, a silicon film containing phosphorus at 1 to 5 x 10<sup>21</sup>  $\text{cm}^{-3}$  concentration, or a multilayered film comprising the silicon film laminated thereon with molybdenum (Mo), tungsten (W),  $\text{MoSi}_2$  or  $\text{WSi}_2$  film was formed. This film was patterned with a third photomask (83) to obtain the configuration shown in FIG. 22(E). A gate electrode 809 was then formed. For example, as a gate electrode, a phosphorus-doped silicon 0.2 $\mu\text{m}$  thick was formed and a molybdenum layer 0.3 $\mu\text{m}$  thick was formed thereon with a channel length of 7 $\mu\text{m}$ .

Also, in the case where aluminum is used as the gate electrode material, after patterning with the third photomask (83), it is possible to form the source and drain contact holes at positions closer to the gate by anodic oxidation of this surface of the patterned aluminum gate electrode so that self-aligning construction can be applied. Therefore, the TFT characteristics can be further increased by improving the mobility and decreasing the threshold voltage.

The entire manufacturing process for the TFT can thus be done without having to apply a temperature above 400°C. This makes it possible to use, as the substrate, materials other than expensive materials such as quartz. Accordingly, this embodiment of the invention is very suitable for a liquid crystal display having a large number of picture elements.



Then, a silicon oxide film was formed as an interlayer insulator 810 by sputtering method. In place of the sputtering method, LPCVD method, photo CVD method, and normal pressure CVD may be utilized for the formation of the silicon oxide film. The thickness of the layer was 0.2 to 0.6 $\mu$ m, for example. After that, an opening 811 for electrode was formed using a forth photomask (84). On the entire surface of this structure, an aluminum film having a thickness of 0.3 $\mu$ m was formed by sputtering method, and then a lead 812 and a contact 813 were formed using a photomask (85). An organic resin for surface-flattering 814, e.g. a transparent polyimide resin was then applied on the top surface, and further an opening for an electrode was again formed using a sixth photomask (86).

An ITO (Indium Tin Oxide) film of 0.1 $\mu$ m thickness was formed on the entire surface of this structure by sputtering and was subsequently patterned into a pixel electrode 815 by using a seventh photomask (87). This ITO film was formed at room temperature to 150°C and annealed at 200°C to 400°C in an oxygen or an atmosphere.

The electrical characteristics of the thus formed TFT were as follows:

Mobility: 80cm<sup>2</sup>/Vs

Vth: 5.0V

In accordance with the foregoing method, the first substrate for a liquid crystal electro-optical device was completed.

The method for forming the second substrate is shown in Fig.23.

A polyimide resin film, made of polyimide mixed with black pigment, having a thickness of 1 $\mu$ m was formed on a glass substrate 500 by spin coat method and was then patterned into

black stripes 501 by the use of a first photomask 411.

Then, a film of polyimide resin mixed with red pigment having a thickness of  $1\mu\text{m}$  was formed by spin coat method and was subsequently patterned into red color filters 502 by the use of a second photomask 412.

In the same manner as the above, green color filters 503 were formed by the use of a third photomask 413, and blue color filters 504 by the use of a fourth photomask 414.

During the formation of the filters, the filters were baked at  $350^{\circ}\text{C}$  for 60 min. in an nitrogen atmosphere.

Subsequently, a transparent polyimide layer was formed as a leveling layer 505 by spin coat method.

On the entire surface of the structure, an ITO film of  $0.1\mu\text{m}$  thickness was formed by sputtering and was patterned into a common electrode 506 by the use of a fifth photomask 415. This ITO film was formed at room temperature to  $150^{\circ}\text{C}$  and annealed at 200 to  $300^{\circ}\text{C}$  in an oxygen or an atmosphere. Thus, the second substrate was completed.

A polyimide precursor material was printed on the above substrates by off-set method and baked at  $350^{\circ}\text{C}$  for 1 hour in an non-oxide atmosphere, e.g. in a nitrogen. Then the surface of the polyimide was subjected to a known rubbing method, so as to provide a means for orienting liquid crystal molecules in a fixed direction in at least an initial stage.

A nematic liquid crystal composition was interposed between the first and second substrates and the periphery of the substrates was sealed with an epoxy adhesive. An drive IC in TAB form and a PCB comprising a common signal wiring and an electric potential wiring were connected to the lead on the substrate, and a polarizing plate was affixed to the outside whereby a light-

transmission type liquid crystal electro-optical device was obtained.

Fig.24 shows the schematic configuration of the electro-optical device obtained in accordance with this embodiment.

The liquid crystal panel 1000 obtained by the above steps was combined with a back light device 1001 comprising three cool cathode tubes. Then a tuner 1002 for receiving TV electric waves was connected thereto, to thereby complete an electro-optical device. Since the electro-optical device thus obtained had a flat form compared with the conventional CRT type electro-optical device, it was possible to hang it on the wall and the like.

Next, the configuration of a peripheral circuitry of the liquid crystal electro-optical device is described with reference to Fig.25.

The peripheral circuitry comprises a driver circuit 1103 connected to information signal side wires 1101 and 1102 which are connected to the matrix circuit of the liquid crystal electro-optical device. The driver circuit 1103 is divided into two drive frequency systems. One of them is a data latch circuit system 1104 having a drive method same as the conventional method, where the main composition is a basic clock CLK1, 1106 for transferring data 1105 by turns and 1 - 12 bits parallel processing is conducted. The other is the system composed in accordance with the present invention, that is, it is composed of a flip flop circuit 1108, a counter 1109 and a clock CLK2, 1107 for the independent frequency from the data transfer frequency. Pulses are formed by the counter 1109 so as to correspond to the gradated display data transmitted from the data latch system 1104.

It is exactly this system which the present invention is

characterized by. That is, by utilizing two kinds of drive frequency, a clear digital gradated display can be obtained without reducing frame numbers for rewriting a picture. Accordingly, occurrence of flicker and the like due to the reduction of the frame number can be avoided.

On the other hand, in a driver circuit 1112 connected to scanning signal lines 1110 and 1111, the electric potential transmitted from a voltage level 1113 is controlled by a flip flop circuit 1115 of a clock CLK 1114 to supply address signals.

In the TFT obtained in accordance with this embodiment the mobility was  $80\text{cm}^2/\text{Vs}$ , so that drive frequency could be increased up to about 1 MHz. Therefore, a gradated display of up to 42 gradations was possible, the gradation number being calculated by the following formula:

$$1 \text{ MHz} / (400 * 60) = 42$$

where 1 MHz represents the drive frequency, 400 the duty number, and 60 the frame number.

In the case of an analogue gradated display method, a gradated display of 16 gradations was its limit due to the variation of the TFT characteristics. In the case of the digital gradated display method of the present invention, however, since the influence from the variation of the TFT characteristics is very little, a gradated display of 42 gradations is possible. In the case of a color display, a colorful, fine display of 74,088 colors is possible.

#### [Embodiment 8]

This embodiment describes the manufacture of a video camera

viewfinder utilizing a liquid crystal electro-optical device of 1 inch diagonal.

In this embodiment, a device utilizing amorphous TFTs in a 387 x 128 matrix by low temperature processing was formed for a viewfinder. The manufacturing method of the liquid crystal display device utilized in this embodiment is explained below with reference to Fig.26.

A silicon oxide film of 1000 to 3000Å thickness was formed as a blocking layer 1201 on inexpensive glass 1200 such as soda-lime glass by magnetron RF (high frequency) sputtering method. The process conditions were as follows:

Atmosphere: 100% oxygen

Film Formation Temperature: 15°C

Output Power: 400 - 800W

Pressure: 0.5 Pa.

Quartz or single-crystal silicon was utilized as a target, and the film formation speed was 30 to 100Å/min.

Then, a silicon film containing a 1 to 5 x 10<sup>21</sup> cm<sup>-3</sup> concentration of phosphorus, or a multilayered film comprising the silicon film laminated thereon with molybdenum (Mo), tungsten (W), MoSi<sub>2</sub> or WSi<sub>2</sub> film was formed, which was then patterned with a first photomask (21) to form a gate electrode 1202 as in Fig.26(A). In this embodiment, the channel length was 10µm and as a gate electrode a phosphorus doped silicon film of 0.2µm thickness was formed and a molybdenum film of 0.3µm thickness was formed further thereon.

In the case of utilizing aluminum (Al) for the gate electrode material, after patterning with the first photomask (21), it is possible to prevent the occurrence of cracks, voids in a channel region or an insulating layer on the gate electrode by

anodic oxidation of this surface of the patterned aluminum gate electrode. Therefore, the TFT characteristics can be further increased by improving mobility and decreasing the threshold voltage.

A silicon oxide film was then formed as a gate insulating film 1203 in the thickness range of 500 to 2000Å, e.g. 1000Å. This was prepared under the same conditions as the silicon oxide film formed as a blocking layer. A small amount of fluorine may be added to this film for fixation of the sodium ions during the film formation.

An amorphous silicon film was then formed on this structure by plasma CVD method. When forming a silicon film by plasma CVD, the temperature was maintained at e.g. 300°C and monosilane ( $\text{SiH}_4$ ) or disilane ( $\text{Si}_2\text{H}_6$ ) was utilized. The gas was introduced into a PCVD apparatus and a high frequency electric power of 13.56MHz was inputted thereto, whereby the film was formed.

With respect to the film formed by the above method, it is preferable that the oxygen concentration is  $5 \times 10^{21} \text{ cm}^{-3}$  or less. If the oxygen concentration is higher than this range, the mobility is decreased. If the concentration is too low, the current leak in the OFF state increases because of the back light. For this reason, the concentration is held in the range from  $4 \times 10^{19}$  to  $4 \times 10^{21} \text{ cm}^{-3}$ . Silicon concentration was assumed to be  $4 \times 10^{22} \text{ cm}^{-3}$ . Hydrogen concentration was  $4 \times 10^{20} \text{ cm}^{-3}$  which is equal to one atomic % of the silicon concentration. In accordance with the above method, a silicon film in an amorphous state was formed to be 500 to 5000Å, e.g. 1500Å thick.

Then, a resist film 1204 for forming a contact region by lift-off method was formed utilizing a second photomask (22), and on the top surface a silicon film 1205 to be an n-type activation

layer was formed by plasma CVD. The film formation temperature was in the range from 250° to 350°C; at 320°C in this embodiment. Monosilane and monosilane-based phosphine ( $\text{PH}_3$ ) at a concentration of 1% and hydrogen ( $\text{H}_2$ ) were introduced at a ratio of 5 : 3 : 20 into a PCVD apparatus at a pressure of 5 Pa and a high frequency electric field at 13.56MHz was applied to form the silicon film. At this moment, a high frequency electric power of 0.05 to 0.20W/cm<sup>2</sup> was appropriate, and an electric power of 0.120W/cm<sup>2</sup> was utilized in this embodiment.

The thus formed silicon film 1205 to be an n-type activation layer had a specific electric conductivity of about  $2 \times 10^{-1} \Omega\text{cm}^{-1}$ . The film thickness thereof was 50Å. Then, aluminum film 1206 of 3000Å thickness was formed for a lead and a contact electrode by sputtering. Unnecessary portions of the aluminum film were removed by lift-off method to form a source region 1207 and a drain region 1208.

After forming each TFT 1209 in the form of island by the use of a third photomask (23), an organic resin 1210 for surface flattening, e.g. a transparent polyimide resin, was applied as shown in Fig.12(D), and an opening for electrode was again formed by the use of a photomask (24).

In order to connect the output end of the NTFT to one of transparent pixel electrodes of the liquid crystal device, an ITO (Indium Tin Oxide) film was formed by sputtering method. The ITO film was subjected to etching by using a photomask (25) to form an electrode 1211. The ITO film was formed at room temperature to 150°C and annealed at 200°C to 400°C in an oxygen or an atmosphere. Thus, an NTFT 1209 and an electrode 1211 made of a transparent conductive film were formed on an identical glass substrate 1200. The electrical characteristics of the thus

obtained TFT were as follows:

Mobility:  $0.2\text{cm}^2/\text{Vs}$

$V_{th}$ : 5.3V.

Next, in the same manner as in Embodiment 7, color filters and a transparent conductive film of ITO were formed to a thickness of 1000Å on an insulating substrate to obtain a second substrate.

On the substrates, a polyimide precursor material was printed by off-set printing and baked at 350°C for 1 hour in a non-oxidation atmosphere, e.g. in nitrogen. The surfaces of the polyimide were then subjected to a known rubbing treatment so as to provide a means for orienting liquid crystal molecules in a fixed direction in at least an initial stage. Thus, the first and second substrates were completed.

Then a nematic liquid crystal composition was interposed between the first and the second substrates, and the periphery thereof was sealed with an epoxy adhesive. Since the pitch of the leads on the substrate was so fine as 46µm, the connection was carried out by the use of COG method. In this embodiment, leads were connected to gold bumps provided on an IC chip by means of a silver paradium resin of epoxy system, and then an epoxy transformed acrylic resin was filled in the space between the substrate and the IC chip for the purpose of fixing and enclosing the IC chip and the substrates. Then a polarizing plate was affixed to the outside thereof, whereby a light-transmission type liquid crystal display device was obtained.

With the TFT in accordance with this embodiment, the mobility of  $0.2\text{cm}^2/\text{Vs}$  could be obtained in spite of the amorphous state, and accordingly the drive frequency could be increased to about 100KHz. Therefore, a gradated display having 13 gradations



was possible, the gradation number being calculated by the following formula:

$$100 \text{ KHz} / (128 * 60) = 13$$

where 100KHz represents a drive frequency, 128 duty number, and 60 a frame number. When carrying out the usual analogue gradated display with a liquid crystal electro-optical device of 50mm square size (the substrate of which size is obtained by dividing 300mm square substrate into 36 plates) on which TFTs of  $384 \times 128 = 49,152$  were formed, the variation of the amorphous TFT characteristic was about  $\pm 10\%$ , so that a gradated display of 8 gradations was its limit. In the case of carrying out the digital gradated display method of the present invention, the method was not affected by the variation of TFT characteristic so much, so that a gradated display of 13 gradations or more was possible. In the case of a color display, a colorful, fine display of 2027 colors was possible.

#### [Embodiment 9]

This embodiment describes the manufacture of a projection type image display device as shown in Fig.27.

In this embodiment, an image projecting part for a projection type image display device was assembled using three liquid crystal electro-optical devices 1300. Each of them had a  $640 \times 480$  dot matrix, and 307,200 pixels were formed within the size of 4 inch diagonal. The size of one pixel was  $127\mu\text{m}$  square.

The projection type image display device is composed of three liquid crystal electro-optical devices 1300 for three primary colors of light, i.e. red, green, and blue respectively, a red color filter 1301, a green color filter 1302, a blue color

filter 1303, reflection boards 1304, a metal halide light source 1307 of 150W, and an optical system for focus 1308.

The substrate of the liquid crystal electro-optical device utilized for an electro-optical device of this embodiment was the one having the NMOS configuration and a matrix circuitry. A device comprising high mobility TFTs formed by low temperature process was utilized to compose the projection type liquid crystal electro-optical device.

The manufacturing method for the liquid crystal display device utilized in this embodiment is explained hereinafter with reference to Fig.28.

A silicon oxide film of 1000 to 3000Å thickness was formed as a blocking layer 1401 on glass 1400 by magnetron RF (high frequency) sputtering as shown in Fig.28(A). The glass was the one which was not expensive unlike quartz glass or so and was resistant to thermal treatment at not higher than 700°C, e.g. about 600°C. The process conditions of the film formation were the same as those for the silicon oxide film as a blocking layer in Embodiment 1.

On the silicon oxide film, a silicon film in an amorphous state was formed to be 500 to 5000Å thick, e.g. 1500Å thick, in the same manner as the case of the silicon film in an amorphous state in Embodiment 1.

As in Embodiment 1, the silicon film in an amorphous state was then annealed at an intermediate temperature of 450°C to 700°C for 12 to 70 hours in a non-oxide atmosphere.

Then the silicon film was subjected to photo etching by the use of a first photomask (31) to form a region 1402 for TFT (having a channel width of 20µm), as shown in Fig.28(A).

A silicon oxide film of 500 to 2000Å thickness, e.g. 1000Å

thickness, was then formed as a gate insulating film 1403. The formation conditions thereof were the same as those for the silicon oxide film as a blocking layer. A small amount of fluorine may be added during the film formation for fixation of sodium ions.

Then, a silicon film containing a  $1 \text{ to } 5 \times 10^{21} \text{ cm}^{-3}$  concentration of phosphorus, or a multilayered film comprising the silicon film laminated thereon with molybdenum (Mo), tungsten (W),  $\text{MoSi}_2$  or  $\text{WSi}_2$  film was formed, which was subsequently patterned with a second photomask (32) to form a gate electrode 1404 as in Fig.28(B). In this embodiment, a channel length was made  $10 \mu\text{m}$ , and as a gate electrode the phosphorus doped silicon of  $0.2 \mu\text{m}$  thickness was formed and further a molybdenum film of  $0.3 \mu\text{m}$  thickness was laminated thereon. In Fig.28(C), phosphorus was added by ion implantation method at a dosage of  $1 \text{ to } 5 \times 10^{15} \text{ cm}^{-2}$  to form a source 1405 and a drain 1406.

In the case of utilizing aluminum (Al) as a gate electrode material, after patterning with the second photomask (32), it is possible to form the source and drain contact holes at positions closer to the gate by anodic oxidation of this surface of the patterned aluminum gate electrode so that self-aligning construction can be applied. Therefore, the TFT characteristics can be further increased by improving the mobility and decreasing the threshold voltage.

Next, heat annealing was again carried out at  $600^\circ\text{C}$  for 10 to 50 hours. Impurities in the source 1405 and the drain 1406 were activated to make the source and drain  $\text{N}^+$  regions. A channel forming region 1407 of semi-amorphous semiconductor was formed below the gate electrode 1404.

The entire manufacturing process for the NTFT can thus be

done without having to apply a temperature above 700°C in spite of the self-aligning system. This makes it possible to use materials other than expensive ones such as quartz for substrates. Accordingly, this embodiment of the invention is very suitable for a liquid crystal display having a large number of pixels.

In this embodiment, the heat annealing process was carried out twice as shown in Figs.28(A) and (C). However, the anneal process of Fig.28(A) may be omitted, depending on the desired characteristics, and followed up with the heat anneal process of Fig.28(C), shortening the manufacturing time. In Fig.28(D), an interlayer insulating layer 1408 was made of silicon oxide film using the sputtering method mentioned above.

This silicon oxide film can, however, be formed using the LPCVD method, photo CVD method or normal pressure CVD method.

The thickness of the insulating layer was e.g. 0.2 to 0.6µm.

Next, using photomask (33), an opening 1409 for the electrodes was formed. Then, a layer of aluminum was formed over the entire structure using the sputtering method, and a lead 1410 and a contact 1411 were formed using photomask (34).

An organic resin film 1412 for surface-flattering, e.g. a transparent polyimide resin film was formed, and an opening for an electrode was formed using photomask (35).

In order to connect the output terminal of the NTFT to the transparent electrode of the pixel of the liquid crystal device, an ITO (Indium Tin Oxide) film was formed by sputtering. The ITO film was etched by the use of a photomask (36) to form an electrode 1413. The ITO film was formed at room temperature to 150°C and annealed at 200 to 400°C in an oxygen or an atmosphere.

Thus, the NTFT 1402 and the electrode 1413 of a transparent

conductive film were formed on an identical glass substrate 1400. The electrical characteristics of the obtained TFT were as follows:

Mobility:  $120\text{cm}^2/\text{Vs}$

$V_{th}$ : 5.0V.

A schematic view of the structure is shown in Fig.29. On the substrate (1500 in Fig.29) mentioned above, a mixture of  $10\mu\text{m}$  thickness was formed by die-cast method, the mixture comprising fumaric acid polymeric resin and nematic liquid crystal both dissolved at a ratio of 65 : 35 in a common solvent, xylene. Then the above structure was heated at  $120^\circ\text{C}$  for 180 min. in a nitrogen atmosphere to remove the solvent, whereby a liquid crystal dispersion layer 1501 was formed. It was found that tact-time could be shortened by making the pressure a bit lower than the atmospheric pressure at the moment.

Then, an ITO film was formed by sputtering to obtain an opposed electrode 1502. This ITO film was formed at room temperature to  $150^\circ\text{C}$ . A transparent silicon resin was then applied to be  $30\mu\text{m}$  thick by printing method and was baked at  $100^\circ\text{C}$  for 30 min. to thereby obtain a liquid crystal electro-optical device.

The configuration and the function of the driver IC utilized in this embodiment is the same as that in Embodiment 7.

When a usual analogue gradated display was carried out with a liquid crystal electro-optical device where 307,200 TFTs in  $640 \times 480$  dot matrix were formed within 300mm square, the variation in TFT characteristics was as large as about  $\pm 10\%$ , so that a gradated display of up to 16 gradations was its limit. In the case of the TFTs formed in this embodiment, however, since the drive frequency can be increased up to 2.5MHz, a gradated display

of up to 86 gradations is possible, the gradation number being calculated by the following formula:

$$2.5\text{MHz} / (480 \times 60) = 86$$

where 2.5MHz represents the drive frequency, 480 the number of scanning lines, and 60 the number of frames.

In the case of the digital gradated display method in accordance with this embodiment, the method is not affected by the variation in TFT characteristics so much, so that a gradated display of 86 gradations is possible. With regard to a color display, a colorful, fine display having 262,144 colors can be obtained.

A conventional television set utilizing a liquid crystal display having 16 gradations is not suitable for displaying a natural landscape, for example a 'lock' of one color, since a hollow (uneven) surface of the 'lock' of one color should be displayed by subtly different colors in order to express a variety of shades of the hollow (uneven) surface in sunshine. However, the gradated display in accordance with the present invention makes it possible to project a picture, e.g. a 'lock' of one color, with variations of fine tone.

This liquid crystal electro-optical device is applicable not only to a front type projection TV as shown in Fig.27 but also a rear type projection TV.

#### [Embodiment 10]

This embodiment shows the manufacture of an electro-optical device for a portable computer utilizing a liquid crystal dispersion type display device of reflection type as shown in Fig.30.

The first substrate utilized in this embodiment was formed by the same steps as in Embodiment 7.

This embodiment will be explained below utilizing the liquid crystal electro-optical device shown in Fig.29.

Fumaric acid polymeric resin and a nematic liquid crystal mixed with a black pigment at 15% were dissolved in a common solvent, xylene at a ratio of 65 : 35. This solution was formed to a thickness of 10 $\mu$ m on the substrate 1500 by die-cast method and was then heated at 120°C for 180 min. in a nitrogen atmosphere to remove the solvent, whereby a liquid crystal dispersion layer 1501 was obtained.

Then, an ITO film was formed by sputtering to obtain an opposed electrode 1502. This ITO film was formed at room temperature to 150°C. Then, a silicon resin of white color of 55 $\mu$ m thickness was applied on the rear surface by printing method and baked at 100°C for 90 min to obtain a liquid crystal electro-optical device.

By utilizing the black pigment as the above, it became possible to display black color displayed when the light was dispersed (i.e. when no electric fields were applied) and also white color when the light was transmitted (i.e. when electric fields were applied), whereby a display as if characters were written on a paper could be obtained.

Alternatively, it was possible to display white color when the light was dispersed and black color when the light was transmitted, without mixing the black pigment. In this case, however, it was necessary to make the rear surface black. A display as if characters were written on a paper could be also obtained.

[Embodiment 11]

This embodiment shows the manufacture of a television set to be hanged on the wall utilizing a liquid crystal display device having the circuit configuration shown in Fig.31. TFTs utilized therein are made of polycrystalline silicon subjected to laser annealing and in stagger type.

Fig. 32 shows the layout of the actual electrodes and the like corresponding to the circuit configuration in Fig.31.

In order to simplify the explanation, the parts corresponding to a 2 x 2 (or less) matrix only are shown therein.

Also, the actual driving signal waveform is shown in Fig. 16. For simplicity, the explanation of the signal waveform is also given for the case of 2 x 2 matrix configuration.

The manufacturing process for a liquid crystal panel utilized in this embodiment is explained with reference to Fig.33.

In Fig.33(A), a silicon oxide film for a blocking layer 651 having a thickness of 1000 to 3000Å was formed on a glass substrate 650, using a magnetron RF (high frequency) sputtering method. The glass substrate 650 was made of inexpensive materials glass capable of withstanding heat treatment up to 700°C, e.g. about 600°C.

The process conditions were the same as those for the silicon oxide film as a blocking layer in Embodiment 7.

On the blocking layer 651, a silicon film 652 in an amorphous state was formed to be 500 to 5000Å thick, e.g. 1000Å thick, in the same manner as that for the silicon film in an amorphous state in Embodiment 7.

As shown in Fig.33(B), a photoresist pattern 653 with source



and drain regions opened was formed using a mask (P1). Then, a silicon film to be an n-type activation layer was formed thereon by plasma CVD method. The film formation temperature was maintained at 250°C to 350°C, specifically 320°C in this embodiment. Monosilane ( $\text{SiH}_4$ ) and monosilane-based phosphine ( $\text{PH}_3$ ) at a concentration of 3% were introduced into a PCVD apparatus at a pressure of 5 Pa and a high frequency electric power at 13.56MHz was inputted thereto, to thereby form the silicon film. A high frequency electric power of 0.05 to 0.20W/cm<sup>2</sup> was appropriate, and a high frequency electric power of 0.120W/cm<sup>2</sup> was inputted in this embodiment. The specific electric conductivity of the n-type silicon film thus obtained was about  $2 \times 10^{-1} \Omega \text{cm}^{-1}$ . The film thickness was 50Å.

On the other hand, a photoresist pattern 654 with source and drain regions opened was formed using a mask (P2), as shown in Fig.33(C). Then, a silicon film to be a p-type activation layer was formed thereon by plasma CVD method. The film formation temperature was maintained at 250°C to 350°C, specifically 320°C in this embodiment. Monosilane ( $\text{SiH}_4$ ) and monosilane-based diborane ( $\text{B}_2\text{H}_6$ ) at a concentration of 2% were introduced into a PCVD apparatus at a pressure of 4 Pa and a high frequency electric power at 13.56MHz was inputted to thereby form the silicon film. A high frequency electric power of 0.05 to 0.20W/cm<sup>2</sup> was appropriate, and a high frequency electric power of 0.080W/cm<sup>2</sup> was inputted in this embodiment. The specific electric conductivity of the p-type silicon film thus obtained was about  $1 \times 10^{-1} \Omega \text{cm}^{-1}$ . The film thickness was 50Å.

Then, source and drain regions 655, 656 and 657, 658 were formed by lift-off method. After that, an island region 663 for an N-channel type thin film transistor and an island region 664

for a P-channel type thin film transistor were formed using a mask (P3) 662.

Subsequently, laser annealing to the source, drain, channel regions and laser doping to the activation layers were carried out simultaneously by the use of XeCl excimer laser in the same way as in Embodiment 7. An electron mobility ( $\mu_e$ ) of 15 to  $300\text{cm}^2/\text{Vsec}$  and a hole mobility ( $\mu_h$ ) of 5 to  $100\text{cm}^2/\text{Vsec}$  can be obtained.

A silicon oxide film of 500 to  $2000\text{\AA}$  thickness, e.g.  $1000\text{\AA}$  thickness, was then formed as a gate insulating film. This was prepared under the same conditions as the silicon oxide film formed as a blocking layer. A small amount of fluorine may be added to this film for fixation of the sodium ions during film formation.

When this operation was completed, a silicon film containing phosphorus at  $1$  to  $5 \times 10^{21} \text{ cm}^{-3}$  concentration, or a multilayered film comprising the silicon film laminated thereon with molybdenum (Mo), tungsten (W),  $\text{MoSi}_2$  or  $\text{WSi}_2$  film was formed, which was patterned with a fourth photomask 669 to obtain the configuration shown in FIG. 33(E). Gate electrodes 666 and 667 were then formed. For example, for gate electrodes a phosphorus-doped silicon layer  $0.2\mu\text{m}$  thick was formed and a molybdenum layer  $0.3\mu\text{m}$  thick was formed thereon with a channel length of  $7 \mu\text{m}$ .

Also, in the case where aluminum is used as the gate electrode material, after patterning with the fourth photomask 669, it is possible to form the source and drain contact holes at positions closer to the gates by anodic oxidation of this surface of the patterned aluminum gate electrode so that self-aligning construction can be applied. Therefore, the TFT characteristics

can be further increased by improving the mobility and decreasing the threshold voltage.

The entire manufacturing process for the C/TFT can thus be done without having to apply a temperature above 400°C. This makes it possible to use, as the substrate, materials other than expensive materials such as quartz. Accordingly, this embodiment of the invention is very suitable for a liquid crystal display having a large picture plane.

In Fig.33(F), a silicon oxide film was formed as an interlayer insulator 668 by sputtering method. In place of the sputtering method, LPCVD method, photo CVD method, and normal pressure CVD may be utilized for the formation of the silicon oxide film. The thickness of the layer was 0.2 to 0.6 $\mu$ m, for example. After that, an opening 679 for electrode was formed using a fifth photomask 670. On the entire surface of this structure, an aluminum film having a thickness of 0.3 $\mu$ m was formed by sputtering method, and then a lead 674 and a contact 673 were formed using a sixth photomask 676.

A silicon oxide film was again formed as an interlayer insulating layer 680 by the above mentioned sputtering method. Instead of the sputtering method, the LPCVD method, photo CVD method, and normal pressure CVD method may be utilized for forming the silicon oxide film. The silicon oxide film was then patterned using a seventh photomask 681. Then, on the entire surface an aluminum film of 0.3 $\mu$ m thickness was formed by sputtering. A lead 683 and a contact 684 were then formed using an eighth photomask 682.

An organic resin for surface-flattering 685, e.g. a transparent polyimide resin was then applied on the top surface, and further an opening for electrode was again formed using a

ninth photomask 686.

An ITO film of 0.1 $\mu$ m thickness was formed on the entire surface of this structure by sputtering and was subsequently patterned into pixel electrodes 688 by the use of a tenth photomask 687. This ITO film was formed at room temperature to 150°C and annealed at 200°C to 400°C in an oxygen or an atmosphere.

The electrical characteristics of the thus formed NTFT and PTFT were as follows:

NTFT ... Mobility: 80cm<sup>2</sup>/Vs

Vth: 5.0V

PTFT ... Mobility: 30cm<sup>2</sup>/Vs

Vth: 5.5V.

In accordance with the foregoing method, the first substrate for a liquid crystal electro-optical device was completed.

A second substrate for the liquid crystal electro-optical device was formed in the same manner as in Embodiment 7.

A nematic liquid crystal composition was interposed between the first and second substrates and the periphery of the substrates was sealed with an epoxy adhesive. An driver IC in TAB form and a PCB comprising a common signal wiring and a potential wiring were connected to the lead on the substrate, and a polarizing plate was affixed to the outside whereby a light-transmission type liquid crystal electro-optical device was obtained.

The structure of the electro-optical device obtained in accordance with this embodiment is the same as that in Embodiment 7 and schematically illustrated in Fig.24.

Next, the configuration of a peripheral circuitry of the liquid crystal electro-optical device is described with reference

to Fig.34.

A driver circuit 352 is connected to information signal side wires 350 and 351 which are connected to the matrix circuit of the liquid crystal electro-optical device. The driver circuit 352 is divided into two drive frequency systems. One of them is a data latch circuit system 353 having a drive method same as the conventional method, where the main composition is a basic clock  $\phi H$  355 for transferring data 356 by turns and 1 - 12 bits parallel processing is conducted. The other is the system composed in accordance with the present invention, that is, it is composed of a magnitude comparator circuit 358, a buffer 360 for panel drive and a clock CLK 357 for the independent frequency of the data transfer frequency. Pulses are formed by the counter 358 so as to correspond to the gradated display data transmitted from the data latch system 353.

It is exactly this system which the present invention is characterized by. That is, by utilizing two kinds of drive frequency, a clear digital gradated display can be obtained without reducing frame numbers for rewriting a picture. Accordingly, occurrence of flicker and the like due to the reduction of the frame number can be avoided.

Fig.35 is a photograph of oscilloscope showing input signal waveforms inputted to and output signal waveforms outputted from the C/TFT obtained in this embodiment. In Figs.35(A) to (D), drive frequency of input signals is raised as 5KHz, 50KHz, 500KHz, and 1MHz. As is apparent from Fig.35(D), even at 1MHz, output signal waveforms do not become gentle so much and fully useful output signals can be obtained.

The number of gradations of a gradated display can be calculated by dividing the drive frequency by duty number and

frame number. In the case of the drive frequency of 1MHz, a gradated display of 42 gradations (calculated by dividing 1MHz by 400 and 60) can be obtained.

In the case of an analogue gradated display method, a gradated display of 16 gradations was its limit due to the variations in TFT characteristics. In the case of the digital gradated display method of the present invention, however, since the method is not affected by the variations in TFT characteristics so much, a gradated display of up to 42 gradations is possible. With regard to a color display, a colorful, fine display of 74,088 colors can be obtained.

#### [Embodiment 12]

This embodiment shows the manufacture of a video camera viewfinder utilizing a liquid crystal electro-optical device of 1 inch diagonal.

In this embodiment, a first substrate with 387 x 128 pixel configuration was prepared by the same process as in Embodiment 11. Also, a second substrate was prepared by providing color filters and a transparent conductive film ITO to a thickness of 1000Å on a substrate made of insulator by the same process as in Embodiment 11.

On the above substrates, a polyimide precursor material was printed by off-set method, and subsequently the substrates were baked at 350°C for 1 hour in a non-oxidizing atmosphere, e.g. in a nitrogen. Then, the surfaces of the polyimide films were subjected to a know rubbing treatment, whereby the first and second substrate provided with means for orientating liquid crystal molecules in one fixed direction in at least an initial

stage were obtained.

A nematic liquid crystal composition was interposed between the above first and second substrates and the periphery of the substrates was sealed with an epoxy adhesive. Since the pitch of the leads on the substrates was as fine as  $46\mu\text{m}$ , connection was conducted by COG method. In this embodiment, leads were connected to gold bumps provided on an IC chip by means of a silver paradium resin of epoxy system, and then an epoxy transformed acrylic resin was filled in the space between the IC chip and the substrates for the purpose of fixing and enclosing the IC chip. Then a polarizing plate was affixed to the outside thereof, whereby a light-transmission type liquid crystal display device was obtained.

Since the channel length was  $5\mu\text{m}$  in the TFT of this embodiment, the drive frequency could be raised up to about 2MHz. Hence, in accordance with the division of 2MHz by 128 and 60, 260 gradations, approximately 256 gradations were possible in a gradated display. When carrying out the usual analogue gradated display with a liquid crystal electro-optical device of 50mm square size (the substrate of which size is obtained by dividing 300mm square-sized substrate into 36 plates) on which TFTs of  $384 \times 128 = 49,152$  were formed, the variation in the amorphous TFT characteristic was about  $\pm 10\%$ , so that a gradated display of 16 gradations was its limit. In the case of carrying out the digital gradated display method of the present invention, the method was not affected by the variation in TFT characteristic so much, so that a gradated display of 256 gradations or more was possible. In the case of a color display, a colorful, fine display of 16,777,216 colors was possible.

[Embodiment 13]

This embodiment describes the manufacture of a projection type image display device as shown in Fig.27.

In this embodiment, an image projecting part for a projection type image display device was assembled using three liquid crystal electro-optical devices 1300. Each of them had a 640 x 480 dot matrix, and 307,200 pixels were formed within the size of 4 inch diagonal. The size of one pixel was 127 $\mu$ m square.

The projection type image display device is composed of three liquid crystal electro-optical devices 1300 for three primary colors of light, i.e. red, green, and blue respectively, a red color filter 1301, a green color filter 1302, a blue color filter 1303, reflection boards 1304, a metal halide light source 1307 of 150W, and an optical system for focus 1308.

The substrate of the liquid crystal electro-optical device utilized for an electro-optical device of this embodiment was the one having C/TFT configuration and a matrix circuitry. A device comprising high mobility TFTs formed by low temperature process was utilized to compose the projection type liquid crystal electro-optical device.

The manufacturing method for the liquid crystal display device utilized in this embodiment is explained hereinbelow with reference to Fig.36.

In Fig.36(A), a silicon oxide film of 1000 to 3000 $\text{\AA}$  thickness was formed as a blocking layer 602 on glass 601 by a magnetron RF (high frequency) sputtering. The glass was the one which was not expensive unlike quartz glass or so and was resistant to thermal treatment at not higher than 700°C, e.g. about 600°C. The process conditions of the film formation were



the same as those for the silicon oxide film as a blocking layer in Embodiment 1.

On the silicon oxide film, a silicon film 603 in an amorphous state was formed to be 500 to 5000Å thick, e.g. 1500Å thick, in the same manner as the case of the silicon film in an amorphous state in Embodiment 1.

As in Embodiment 1, the silicon film in an amorphous state was then heat-annealed at an intermediate temperature of 450° to 700°C for 12 to 70 hours in a non-oxide atmosphere.

A silicon oxide film 604 of 500 to 2000Å thickness, e.g. 1000Å thickness, was then formed as a gate insulating film. The formation conditions thereof were the same as those for the silicon oxide film as a blocking layer. A small amount of fluorine may be added during the film formation for fixation of sodium ions.

Then, a silicon film containing a  $1 \text{ to } 5 \times 10^{21} \text{ cm}^{-3}$  concentration of phosphorus, or a multilayered film comprising the silicon film laminated thereon with molybdenum (Mo), tungsten (W),  $\text{MoSi}_2$  or  $\text{WSi}_2$  film was formed, which was subsequently patterned with a first photomask (41) as in Fig.36(B). In this embodiment, a molybdenum film was formed to a thickness of 0.3µm as a gate electrode with a channel length of 10µm. In the patterning, the gate electrodes were overetched 77 at about 3µm. Then, a positive photoresist 607 was applied on the entire surface of the substrate.

After the application, exposure and development were carried out from the rear side of the substrate, using a photomask (42) to thereby obtain a resist 608. Then, an n-type layer was deposited by sputtering. By subsequently removing the resist 608 by lift-off method, the configuration shown in Fig.36(D) was

obtained.

In the same manner, after a positive photoresist was applied on the entire surface of the substrate, exposure and development were carried out from the rear side of the substrate using a photomask (43) to thereby obtain a resist 610. Then a p-type layer was deposited by sputtering. By removing the resist 610 by lift-off method, the configuration shown in Fig.36(E) was obtained.

The substrate was again heat-annealed at 600°C for 10 to 50 hours, whereby impurities in sources 612, 614 and drains 613, 615 were activated to be N<sup>+</sup> or P<sup>+</sup> type. Channel formation regions 618 and 619 of semi-amorphous semiconductor was formed below gate electrodes 616 and 617.

The entire manufacturing process for the C/TFT can thus be done without having to apply a temperature above 700°C in the self-aligning system. This makes it possible to use materials other than expensive ones such as quartz as the substrate material. Accordingly, this embodiment of the invention is very suitable for a liquid crystal display having a large picture plane.

The heat anneal process, shown in fig.36(A) and Fig.36(E), was performed twice. However, the anneal process in Fig.36(A) can be omitted, depending on the desired characteristics, and followed up with the heat anneal process of Fig.36(E), shortening the manufacturing time.

In Fig.36(F), a silicon oxide film was formed as an interlayer insulator 620 by the sputtering method mentioned above. This silicon oxide film may be formed by the LPCVD method, photo CVD method, or normal pressure CVD method, instead. The thickness of the insulator was e.g. 0.2 to 0.6μm. Next,

using a photomask (44), openings 621 for the electrodes were formed. Then, a layer of aluminum was formed on the entire structure using the sputtering method, and a lead 622 and a contact 623 were formed using a photomask (45), as shown in Fig.36(F).

An organic resin film 624 for surface-flattering, e.g. a transparent polyimide resin film was formed, and electrode an opening for an electrode was provided using a photomask (46).

In order to connect the output terminal of the C/TFT to the (transparent) electrode of the pixel of the liquid crystal display device, an ITO film was formed by sputtering.

The electrode 625 was completed by etching through a photomask (47).

This ITO film was formed in the range from room temperature to 150°C and annealed at 200°C to 400°C in oxygen or atmosphere. The NTFT 626, PTFT 627, and the transparent electrode 625 were thus prepared on an identical glass substrate 601.

The electrical characteristics of the TFTs thus obtained are as follows:

NTFT ... Mobility:  $120\text{cm}^2/\text{Vs}$

$V_{th}$ : 5.0V

PTFT ... Mobility:  $50\text{cm}^2/\text{Vs}$

$V_{th}$ : 5.3V.

The substrate 1500 shown in Fig.29 was obtained by the foregoing process.

A liquid crystal dispersion layer 1501 was formed on the substrate 1500 in the same manner as in Embodiment 9, as shown in Fig.29. Further an opposed electrode 1502 was formed thereon as in Embodiment 9. Then, a transparent silicon resin of 30 $\mu\text{m}$  thickness was applied on the top surface of the structure by

printing method and was baked at 100°C for 30 min. to thereby obtain a liquid crystal electro-optical device.

The configuration and the function of the driver IC utilized in this embodiment are the same as in Embodiment 11.

When a usual analogue gradated display was carried out with a liquid crystal electro-optical device where 307,200 TFTs in 640 x 480 dot matrix were formed within 300mm square, the variation in TFT characteristics was as large as about  $\pm 10\%$ , so that a gradated display of up to 16 gradations was its limit. In the case of the TFTs formed in this embodiment, however, since the drive frequency can be increased up to 2.5MHz, a gradated display of up to 86 gradations is possible, the gradation number being calculated by the following formula:

$$2.5\text{MHz} / (480 \times 60) = 86$$

where 2.5MHz represents the drive frequency, 480 the number of scanning lines, and 60 the number of frames.

With regard to a color display, a colorful, fine display having 262,144 colors can be obtained.

This liquid crystal electro-optical device is applicable not only to a front type projection TV shown in Fig.27 but also to a rear type projection TV.

[Embodiment 14]

This embodiment shows the manufacture of an electro-optical device for a portable computer utilizing a liquid crystal dispersion type display device of reflection type as in Fig.30.

A first substrate 1500 utilized in this embodiment was formed in the same manner as in Embodiment 11.

As shown in Fig.29, a liquid crystal dispersion layer 1501,

a counter electrode 1502 on the layer 1501, and a transparent silicon resin on the electrode 1502 were provided on the substrate 1500 as in Embodiment 10. The silicon resin was subsequently baked at 100°C for 90 min. to thereby obtain a liquid crystal electro-optical device.

In the present invention, a gradated display is provided using a display drive system with the display timing related to the unit time  $t$  for writing-in a picture element and to the time  $F$  for writing-in one picture, wherein, by time-sharing the signal during a write-in of time  $t$ , without changing the time  $F$ , a clear gradated display controlled by digital can be obtained. Compared with the gradated display method using a plurality of frames, a display of high quality is possible without the decrease of display frequency by the digital gradated display method of the present invention.

Instead of a conventional analogue gradated display, the present invention provides a digital gradated display with two kinds of drive frequencies being independent of each other. In the case of utilizing a liquid crystal electro-optical device in 640 x 400 dot matrix, conventionally it was very difficult to form all the 256,000 TFTs without variations in characteristic, and taking the actual productivity and yields into consideration a gradated display of 16 gradations was its limit. On the other hand, in order to make clear the applied voltage level, a reference voltage value is inputted, instead of an analogue value, as a signal from the controller side in the present invention. By controlling by a digital value the timing to connect the reference signal to TFT, the voltage applied to the TFT is controlled, whereby the variation in TFT characteristics is covered. Hence, a clear digital gradated display is possible



WHAT IS CLAIMED IS:

1. An electro-optical device comprising:

a pair of substrates;

an electro-optical modulating layer provided between said substrates;

matrix lines comprising column control lines and row control lines provided on one of said substrates;

a plurality of pixel electrodes provided on said one of said substrates;

a plurality of transistors provided on said one of said substrates, each of the transistors being connected to corresponding one of said pixel electrodes at one of source and drain terminals thereof, to corresponding one of said row control lines at the other one of the source and drain terminals, and to corresponding one of said column control lines at a gate terminal thereof;

means for supplying a signal to each of said transistors at two signal levels of a reference voltage level and an intermediate level;

means for addressing said transistors once per an addressing period;

means for controlling a ratio (a total period of the reference voltage level during the addressing period)/(a total period of the intermediate level during the addressing period);  
and

means for supplying said reference voltage level at high and low two levels with said intermediate level between said high and low two levels, and with said high and low two levels alternated.

2. The device of claim 1 wherein said addressing means can address the row control lines rotationally.

3. The device of claim 1 further comprising:

a first clock for producing a first period; and

a second clock for producing a second period,

wherein one duration of the reference voltage level can be a natural-number times of said first period and one duration of the intermediate level can be a natural-number times of said first period and said addressing period can be two or more natural-number times of said first period and said high and low two levels can be alternated at said second period.

4. The device of claim 1 wherein said electro-optical modulating layer comprises a liquid crystal selected from the group consisting of a ferroelectric liquid crystal, an anti-ferroelectric liquid crystal, a nematic liquid crystal and a cholesteric liquid crystal.

5. The device of claim 1 wherein said electro-optical modulating layer comprises an organic resin and a liquid crystal dispersed in said organic resin, said liquid crystal being selected from the group consisting of a nematic liquid crystal, a cholesteric liquid crystal and a smectic liquid crystal.

6. The device of claim 3 wherein said second period is longer than said first period.

7. The device of claim 3 further comprising means for synchronizing the production of said second period with the



production of the first period with said second period being two or more natural-number times of said first period.

8. The device of claim 1 wherein an offset voltage can be applied to an electrode provided on the other one of said substrates.

9. An electro-optical device comprising:

a pair of substrates;

an electro-optical modulating layer provided between said substrates;

matrix lines comprising column control lines and row control lines provided on one of said substrates;

a plurality of pixel electrodes provided on said one of said substrates;

p-channel and n-channel transistor pairs provided on said one of said substrates, each pair of the p-channel and n-channel transistors being connected to corresponding one of said pixel electrodes at one of source and drain terminals of the p-channel transistor of said each pair and at one of source and drain terminals of the n-channel transistor of said each pair, to one of corresponding pair of the row control lines at the other one of the source and drain terminals of the p-channel transistor, to the other one of said corresponding pair of the row control lines at the other one of the source and drain terminals of the n-channel transistor, and to corresponding one of said column control lines at gate terminals of the p-channel and n-channel transistors of said each pair;

means for supplying a signal to each of said p-channel and n-channel transistor pairs at two signal levels of a

reference voltage level and an intermediate level;

means for addressing said p-channel and n-channel transistor pairs once per an addressing period;

means for controlling a ratio (a total period of the reference voltage level during the addressing period)/(a total period of the intermediate level during the addressing period);  
and

means for supplying said reference voltage level at high and low two levels with said intermediate level between said high and low two levels, and with said high and low two levels alternated.

10. The device of claim 9 wherein said addressing means can address the row control lines rotationally.

11. The device of claim 9 further comprising:

a first clock for producing a first period; and

a second clock for producing a second period,

wherein one duration of the reference voltage level can be a natural-number times of said first period and one duration of the intermediate level can be a natural-number times of said first period and said addressing period can be two or more natural-number times of said first period and said high and low two levels can be alternated at said second period.

12. The device of claim 9 wherein said electro-optical modulating layer comprises a liquid crystal selected from the group consisting of a ferroelectric liquid crystal, an anti-ferroelectric liquid crystal, a nematic liquid crystal and a cholesteric liquid crystal.

13. The device of claim 9 wherein said electro-optical modulating layer comprises an organic resin and a liquid crystal dispersed in said organic resin, said liquid crystal being selected from the group consisting of a nematic liquid crystal, a cholesteric liquid crystal and a smectic liquid crystal.

14. The device of claim 9 further comprising red, green and blue color filter films provided on the other one of said substrates.

15. The device of claim 11 wherein said second period is longer than said first period.

16. The device of claim 11 further comprising means for synchronizing the production of said second period with the production of the first period with said second period being two or more natural-number times of said first period.

17. The device of claim 9 wherein an offset voltage can be applied to an electrode provided on the other one of said substrates.

18. An electro-optical device comprising:

a pair of substrates;

an electro-optical modulating layer provided between said substrates;

a plurality of pixels arranged between said substrates in the form of matrix;

means for addressing said pixels once per an addressing period;

means for supplying digital data to said pixels by the use of two signal levels of a reference voltage level and an intermediate level;

means for controlling a ratio (a total period of the reference voltage level during the addressing period)/(a total period of the intermediate level during the addressing period); and

means for supplying said reference voltage level at high and low two levels with said intermediate level between said high and low two levels, and with said high and low two levels alternated.

19. The device of claim 18 wherein said electro-optical modulating layer comprises a liquid crystal selected from the group consisting of a ferroelectric liquid crystal, an anti-ferroelectric liquid crystal, a nematic liquid crystal and a cholesteric liquid crystal.

20. The device of claim 18 wherein said electro-optical modulating layer comprises an organic resin and a liquid crystal dispersed in said organic resin, said liquid crystal being selected from the group consisting of a nematic liquid crystal, a cholesteric liquid crystal and a smectic liquid crystal.

[illegible][illegible]

# DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO.  
0756-692

PLEASE NOTE:  
YOU MUST  
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FOLLOWING:

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: \* ELECTRO-OPTICAL DEVICE

Insert Title

\_\_\_\_\_, the specification of which is attached hereto unless the following box is checked:

Check Box If  
Appropriate  
For Use Without  
Specification  
Attached

☒ The specification was filed on February 18, 1992  
and was assigned Serial No. 07/837,394  
(if known)  
and was amended on \_\_\_\_\_  
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows:

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and checked at right:

Prior Foreign Application(s)	Priority Claimed
3-77317 (Number) JAPAN (Country) Feb. 16, 1991 (Month/Day/Year Filed)	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
3-77320 (Number) JAPAN (Country) Feb. 16, 1991 (Month/Day/Year Filed)	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
3-77321 (Number) JAPAN (Country) Feb. 16, 1991 (Month/Day/Year Filed)	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
3-87776 (Number) JAPAN (Country) March 27, 1991 (Month/Day/Year Filed)	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
3-89540 (Number) JAPAN (Country) March 27, 1991 (Month/Day/Year Filed)	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months Prior To The Filing Date of This Application:

Country	Application No.	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status—patented, pending, abandoned)

\*NOTE: Must be completed.

I hereby appoint the following attorneys to prosecute this application and/or an international application and to transact all business in the Patent and Trademark Office connected therewith:

Daniel W. Sixbey (Reg. No. 20,932)  
 Stuart J. Friedman (Reg. No. 24,312)  
 Charles M. Leedom, Jr. (Reg. No. 26,477)

Gerald J. Ferguson, Jr. (Reg. No. 23,016)  
 David S. Safran (Reg. No. 27,997)  
 Thomas W. Cole (Reg. No. 28,290)

Send Correspondence to:

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 FOLLOWING

SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.  
 2010 Corporate Ridge, Suite 600  
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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The undersigned hereby authorize any U. S. attorney or agent named herein to accept and follow instructions from \_\_\_\_\_ as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U. S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys or agents named herein will be so notified by the undersigned.

Insert Full Name of First or Sole Inventor and Date This Document is Signed	GIVEN NAME Masaaki HIROKI	FAMILY NAME	INVENTOR'S SIGNATURE <i>Masaaki Hiroki</i>	DATE 3/11/ 1992
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Insert Post Office Address	POST OFFICE ADDRESS (Complete Street Address including City, State & Country) 533-10, Shirane Isehara-shi, Kanagawa-ken 259-11 Japan			
Full Name of Second Inventor, if any: see above	GIVEN NAME Akira MASE	FAMILY NAME	INVENTOR'S SIGNATURE <i>Akira Mase</i>	DATE 3/12/ 1992
	RESIDENCE (City, State & Country) Aichi Japan			CITIZENSHIP Japanese
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country) 3-75-3, Iga-cho, Okazaki-shi, Aichi-ken 444 Japan			
Full Name of Third Inventor, if any: see above	GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE
	RESIDENCE (City, State & Country)			CITIZENSHIP
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country)			
Full Name of Fourth Inventor, if any: see above	GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE
	RESIDENCE (City, State & Country)			CITIZENSHIP
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country)			

Fig. 1

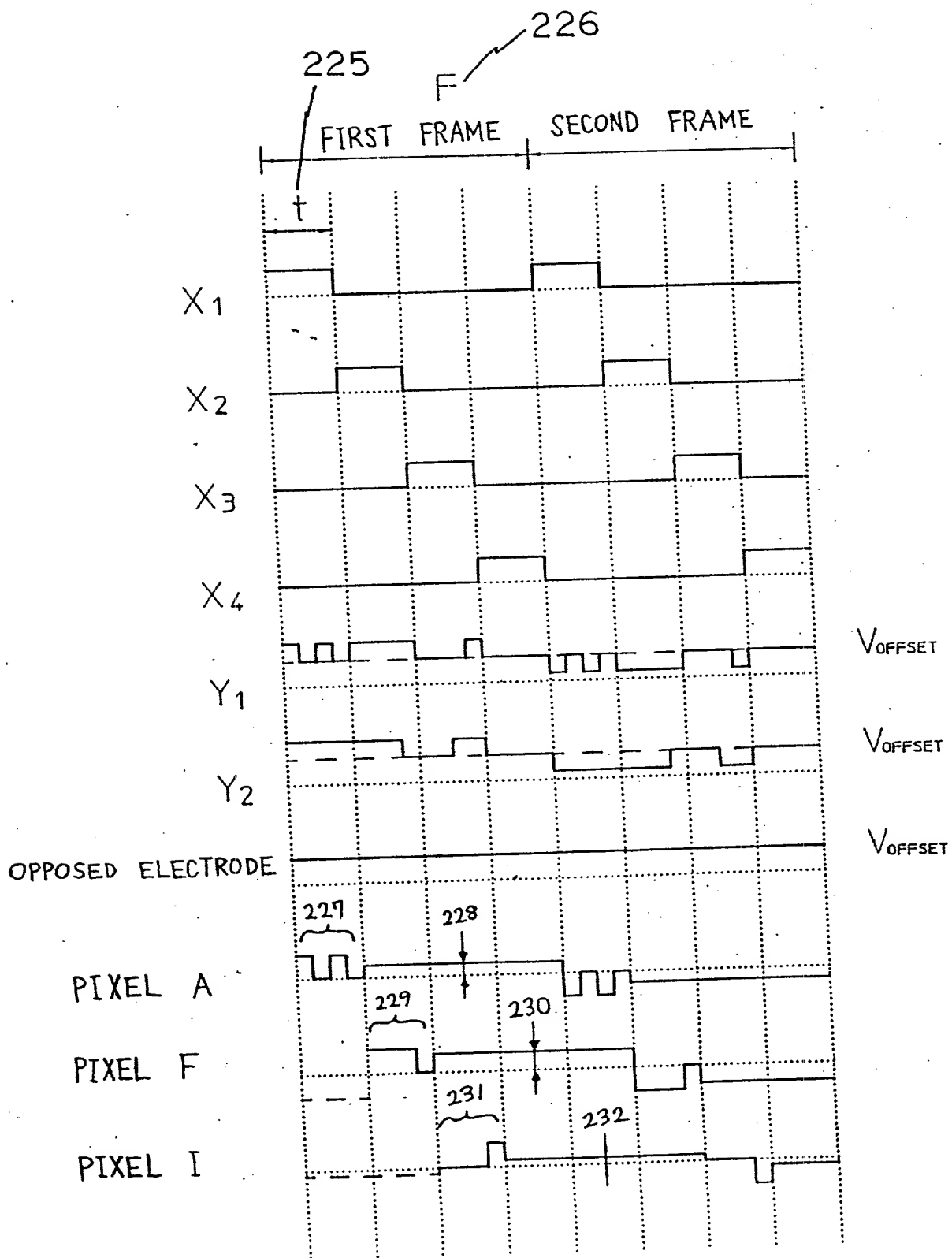




Fig. 2

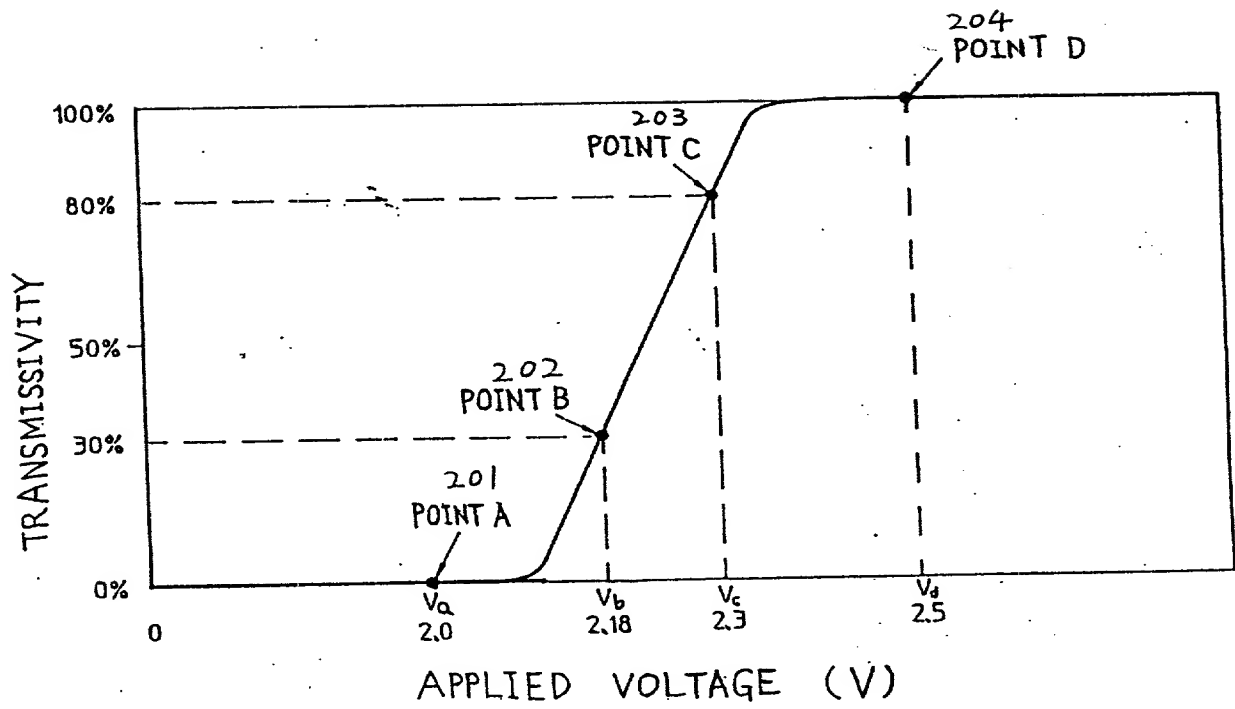
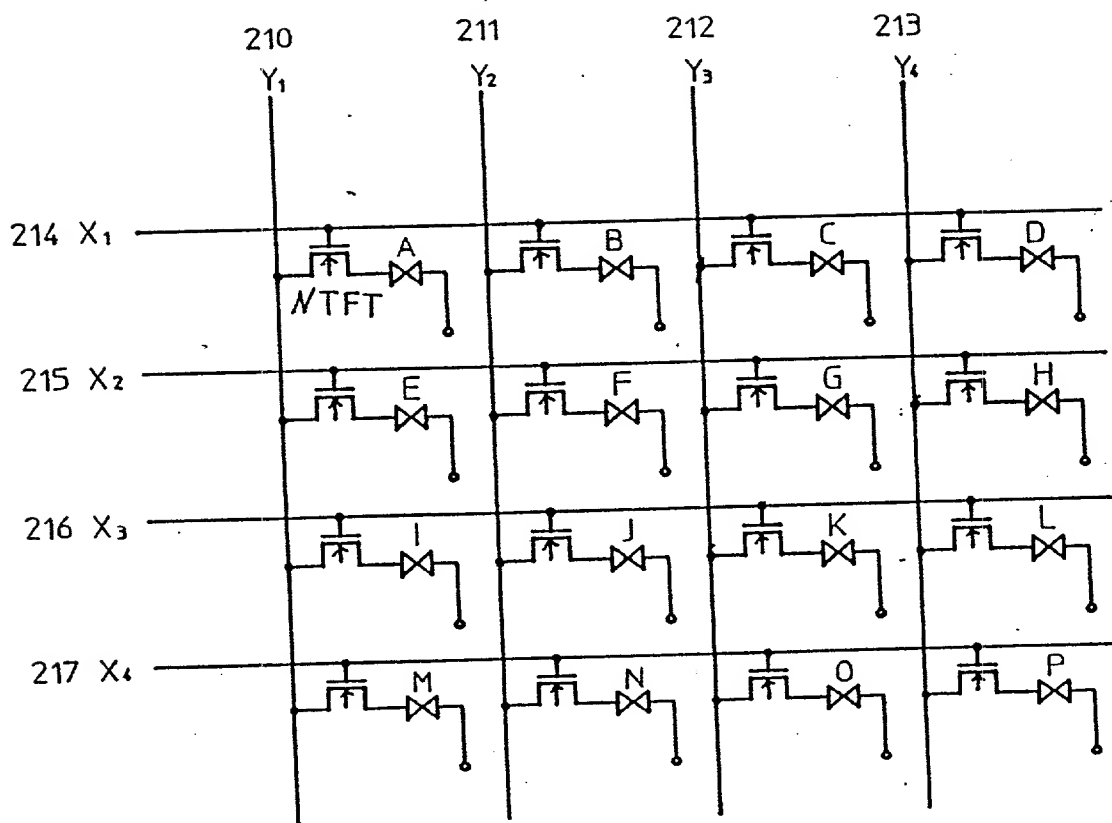


Fig. 3



# Fig. 4

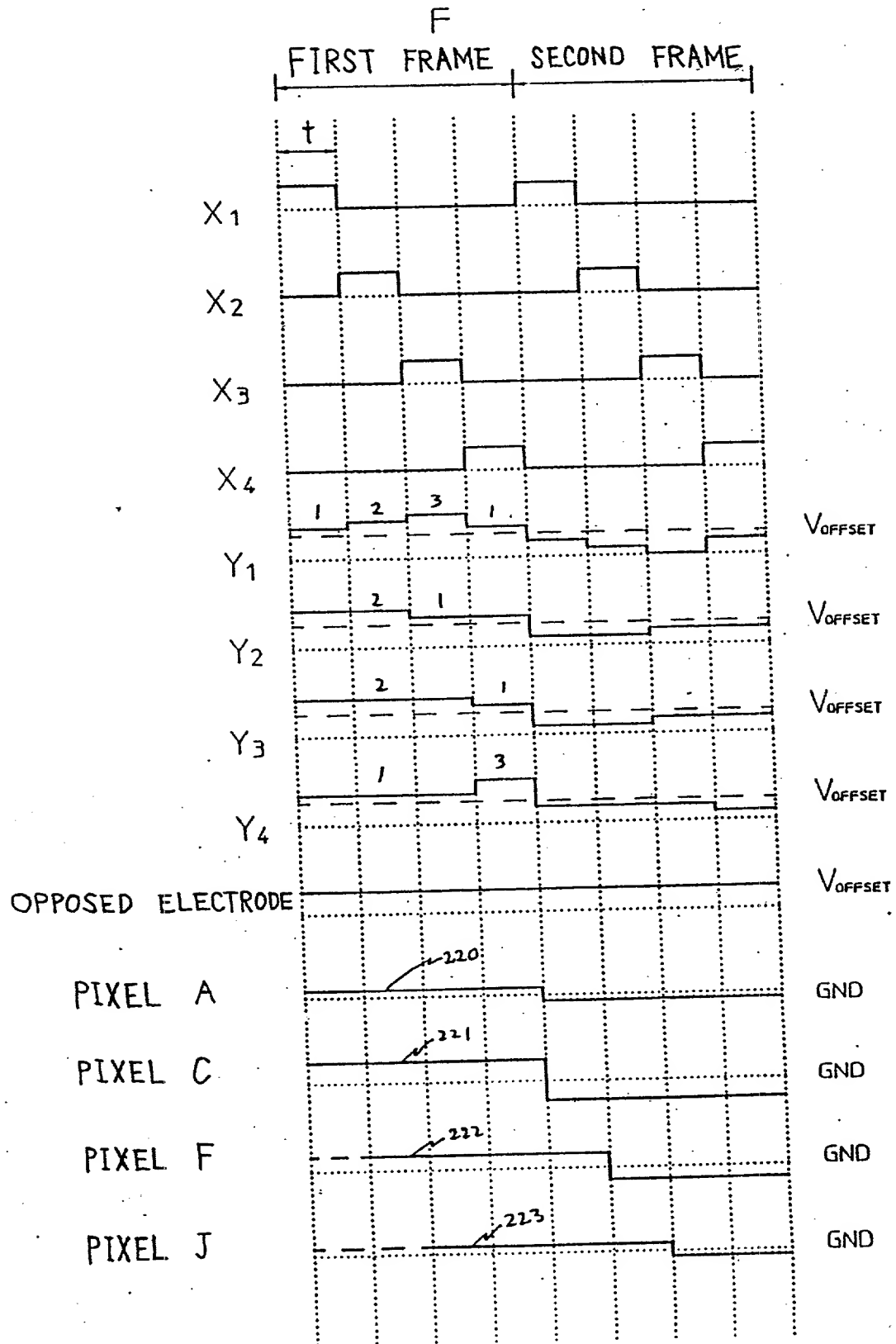


Fig. 5

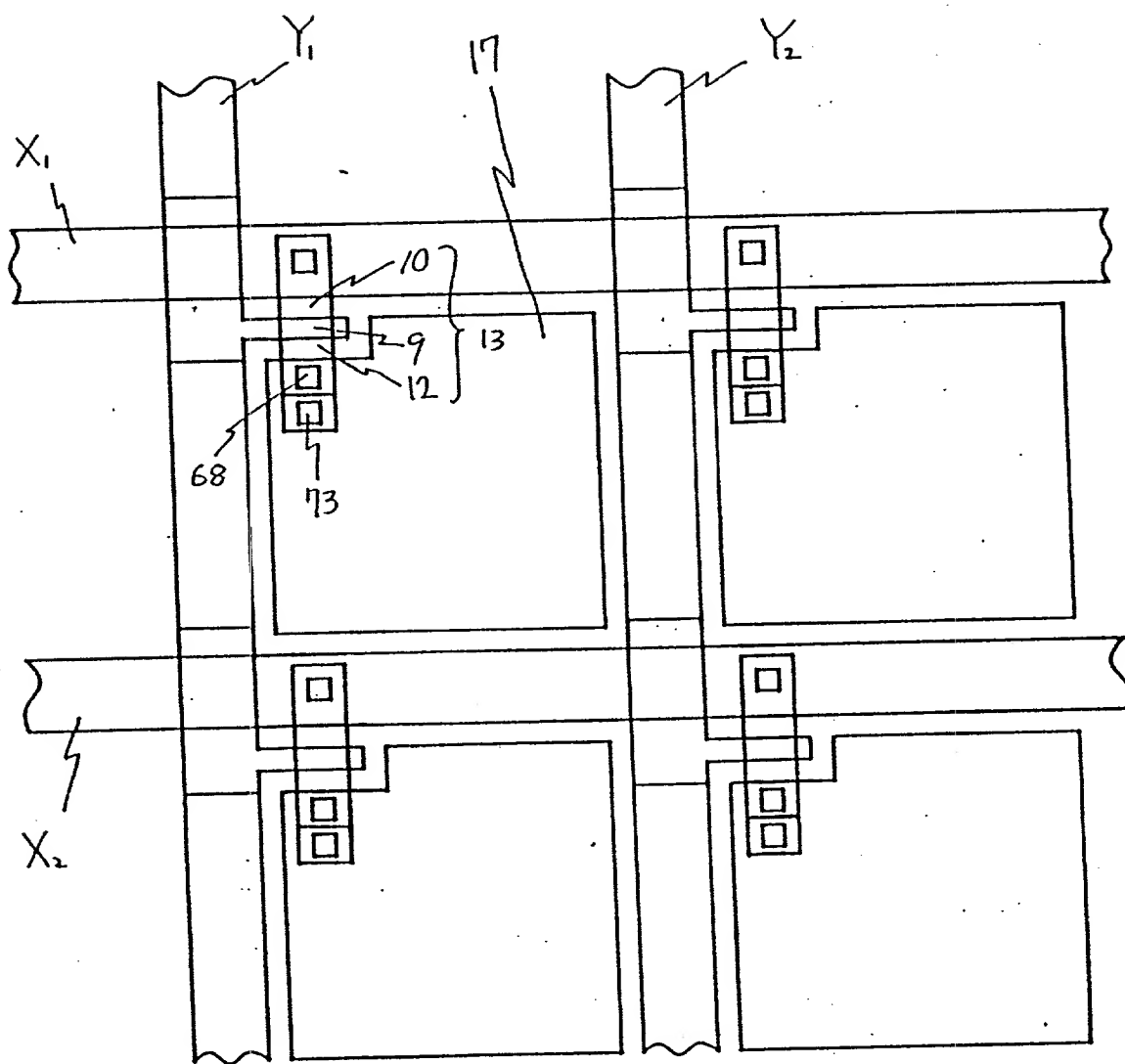


Fig. 6

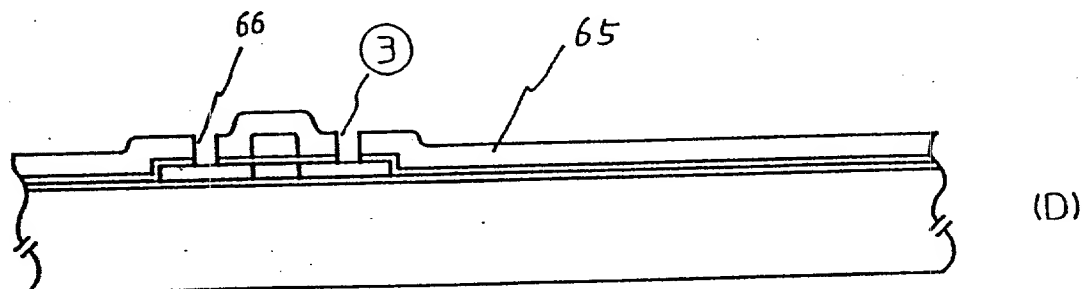
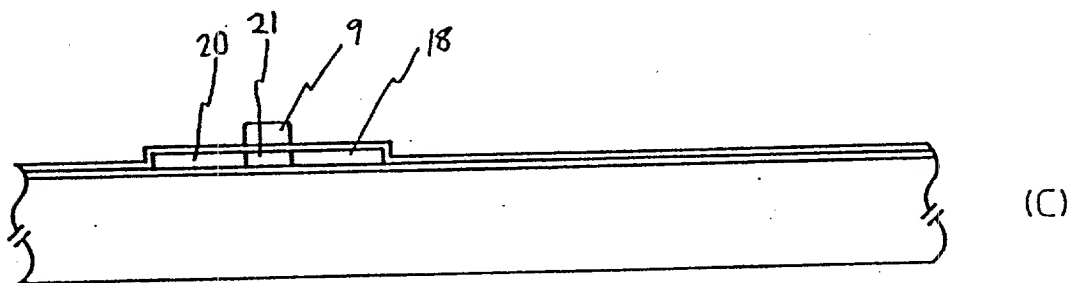
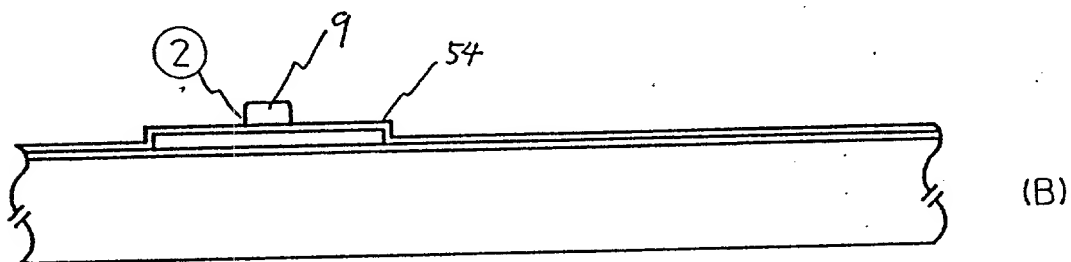
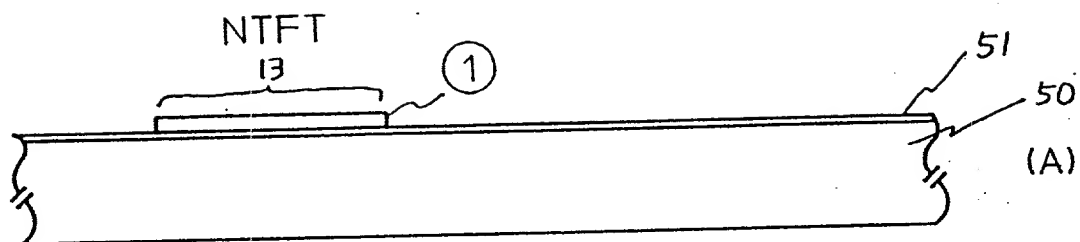


Fig. 6

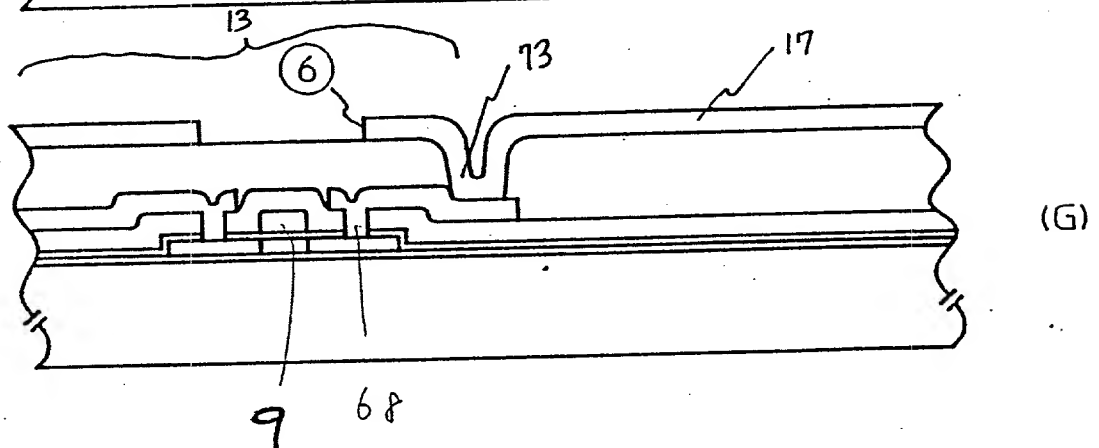
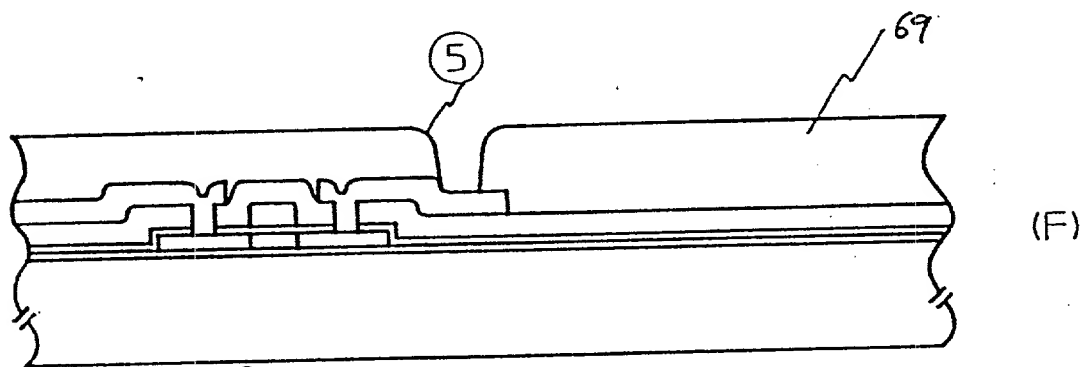
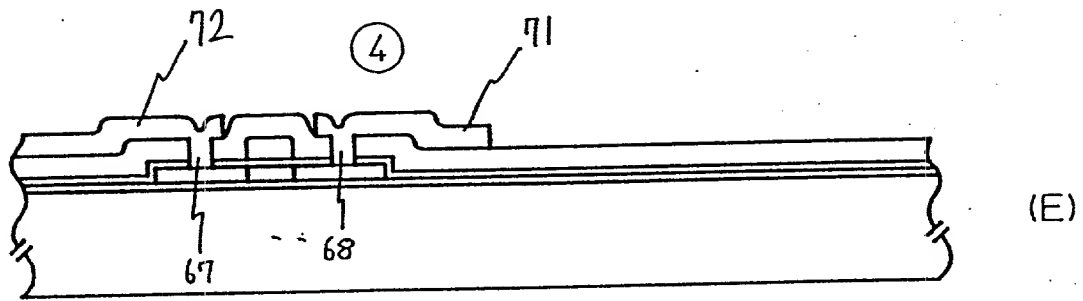
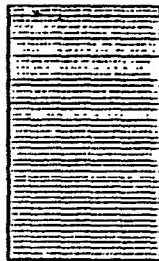
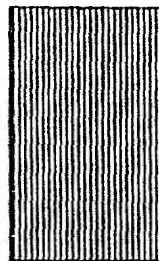


Fig. 7

PIXEL A



PIXEL F



PIXEL I

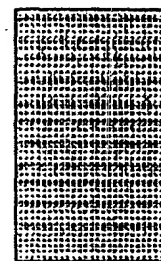
[illegible]

Fig. 8

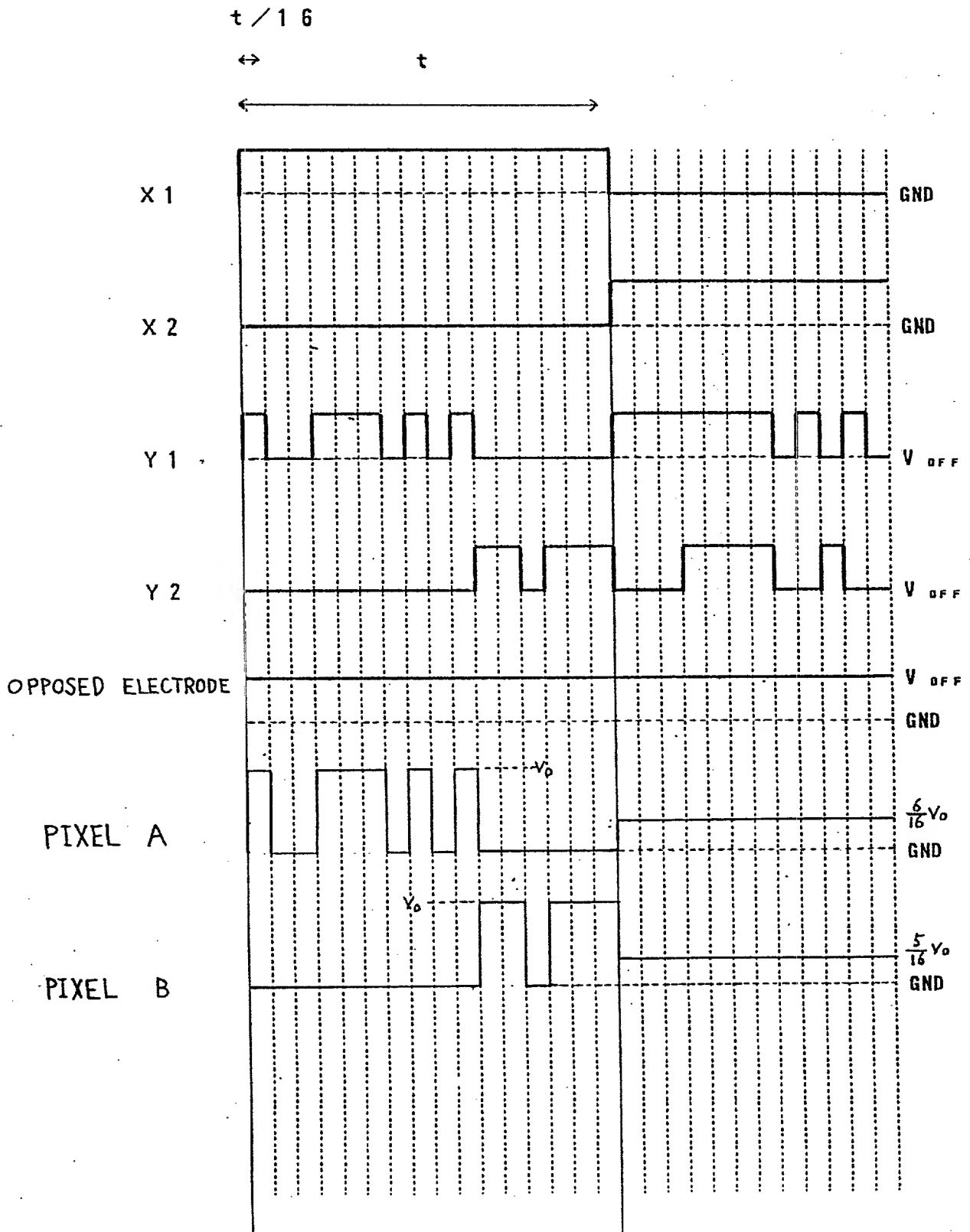




Fig. 9

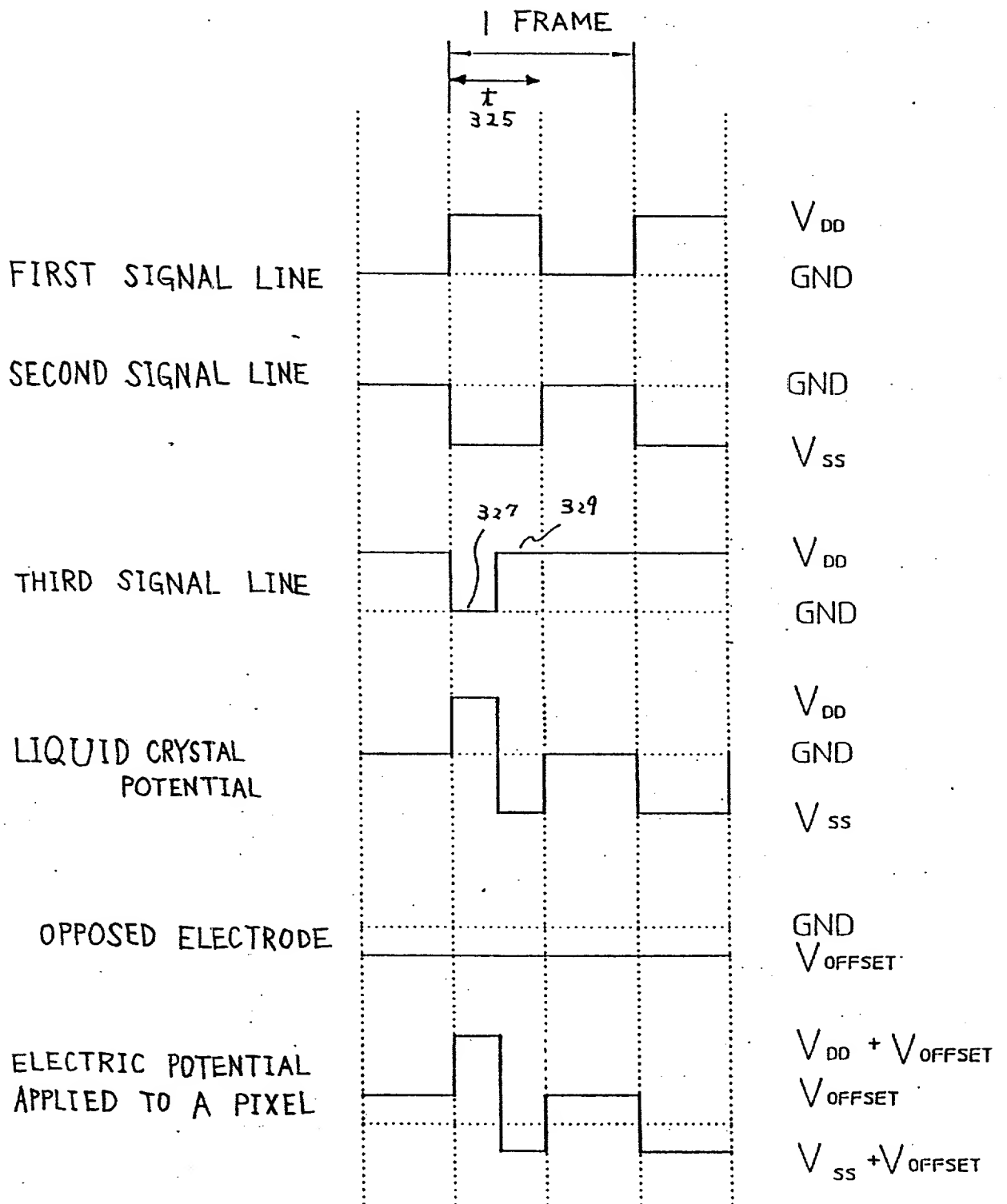


Fig. 10

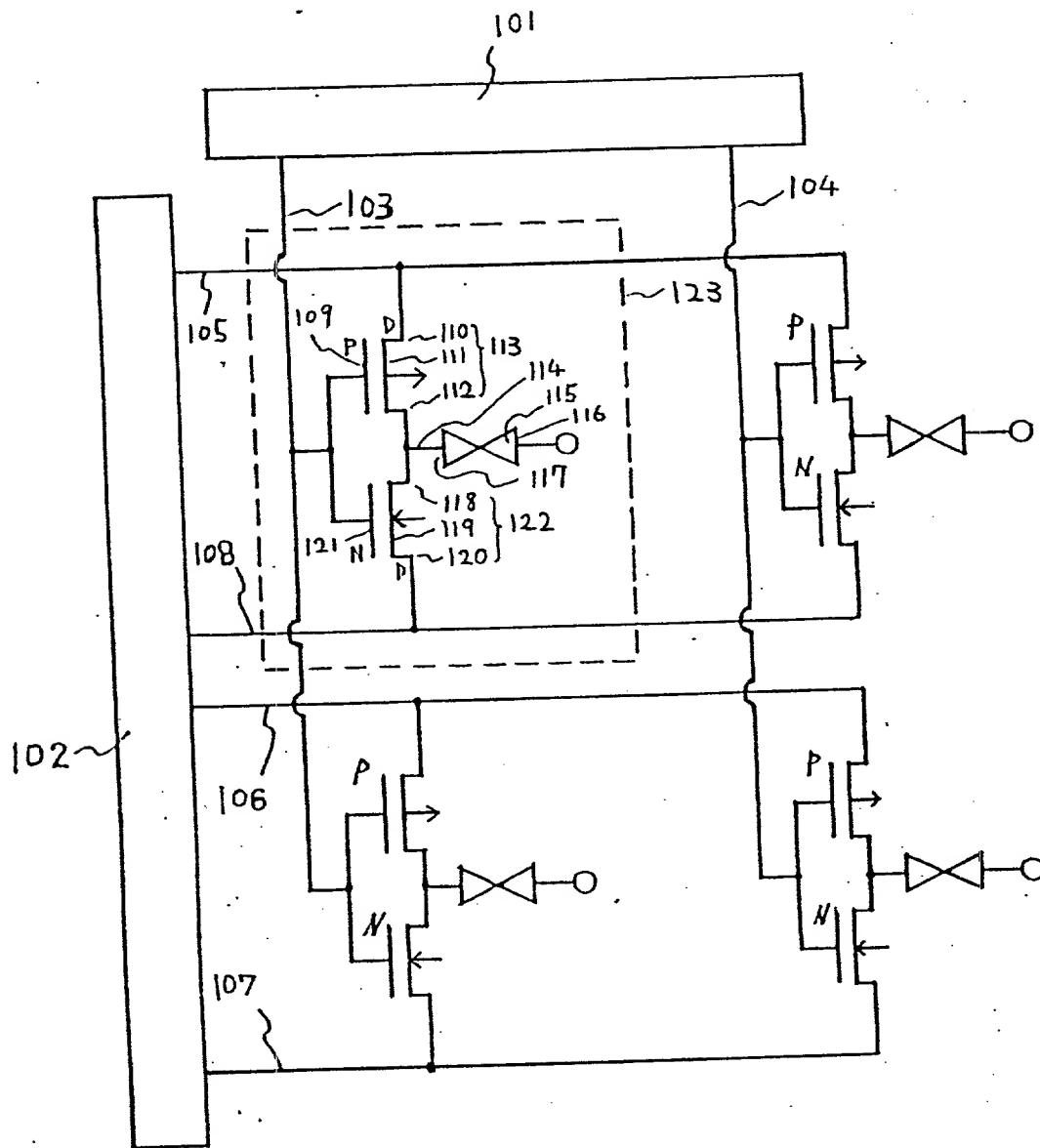


Fig. 11

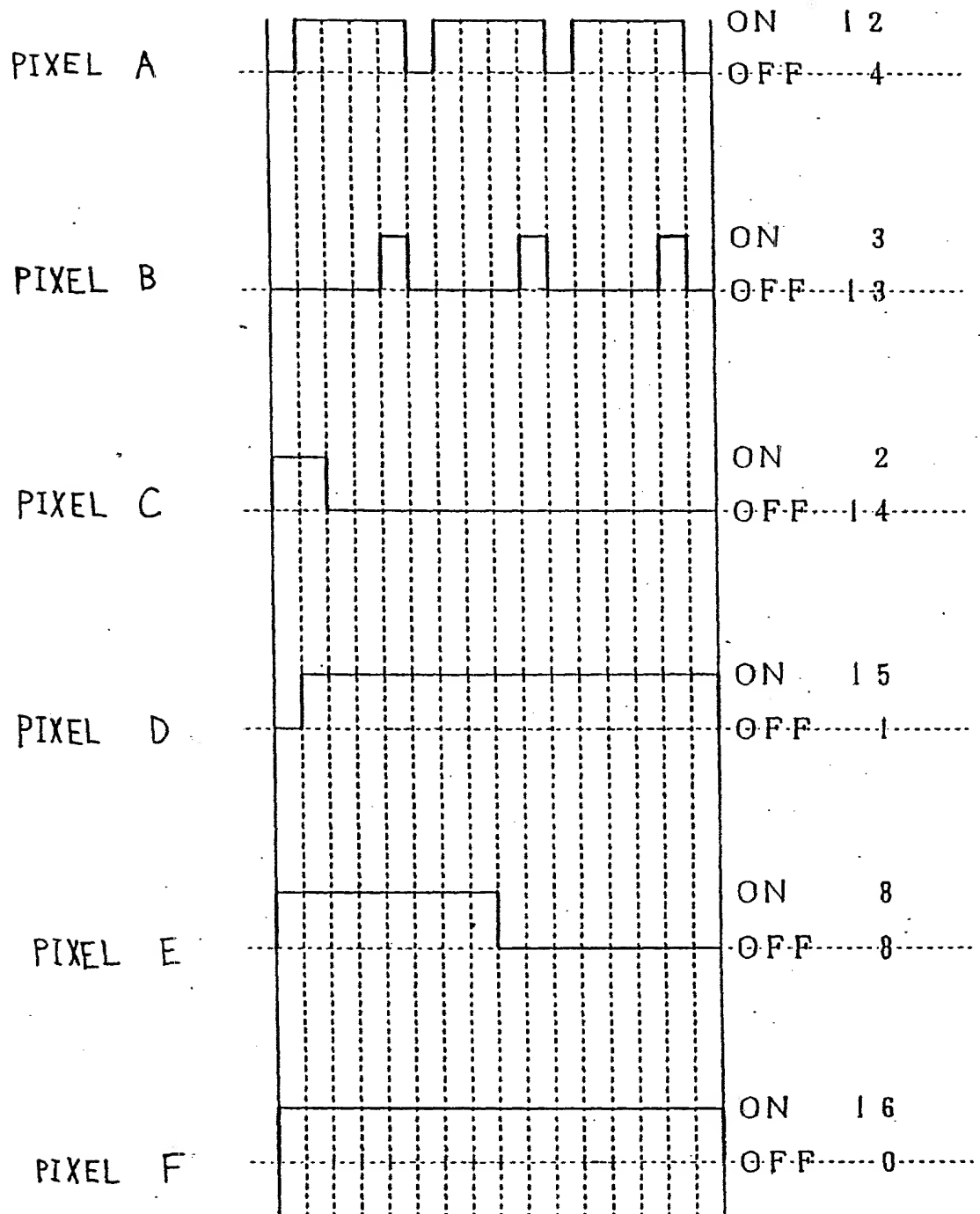


Fig. 12

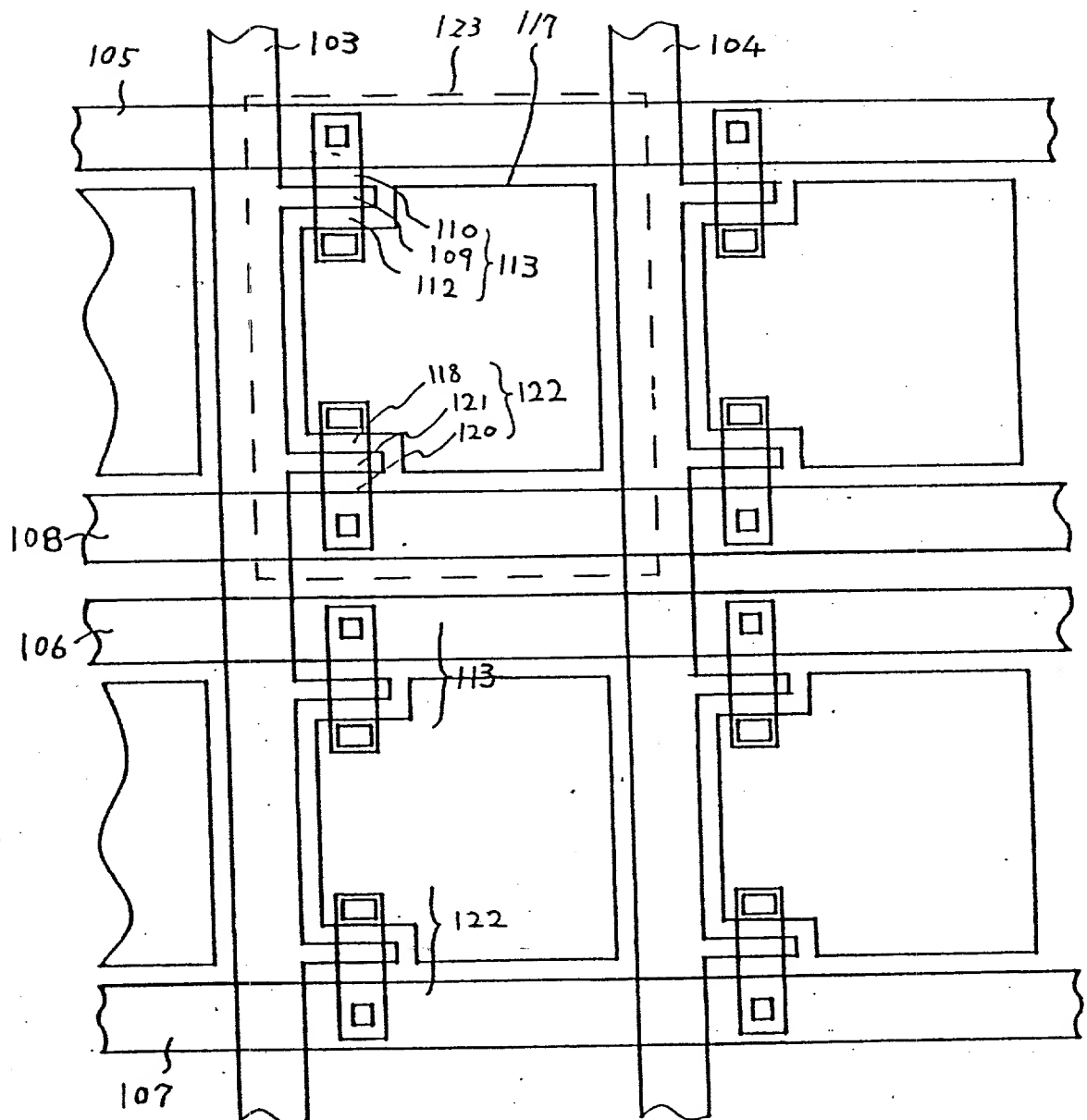


Fig. 13

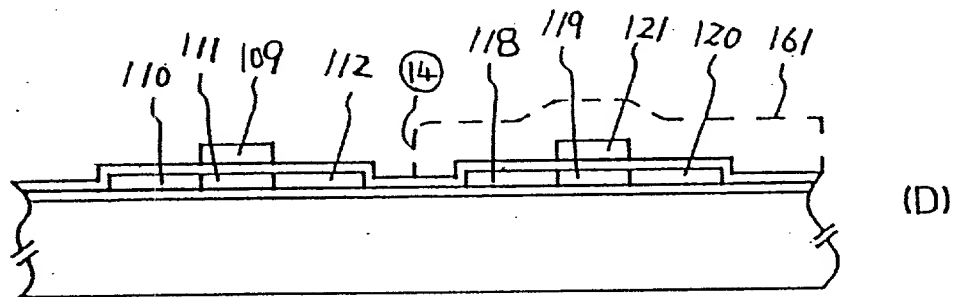
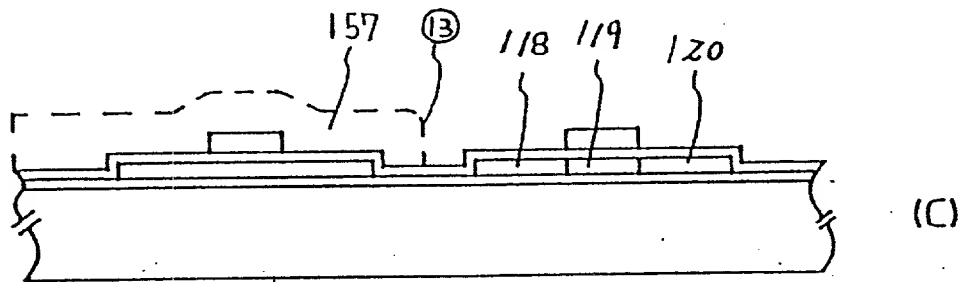
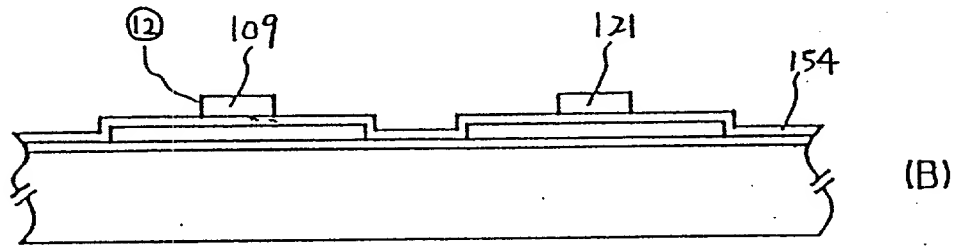
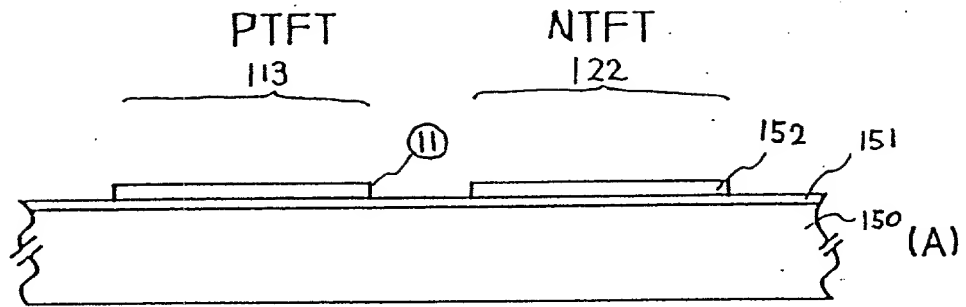


Fig. 13

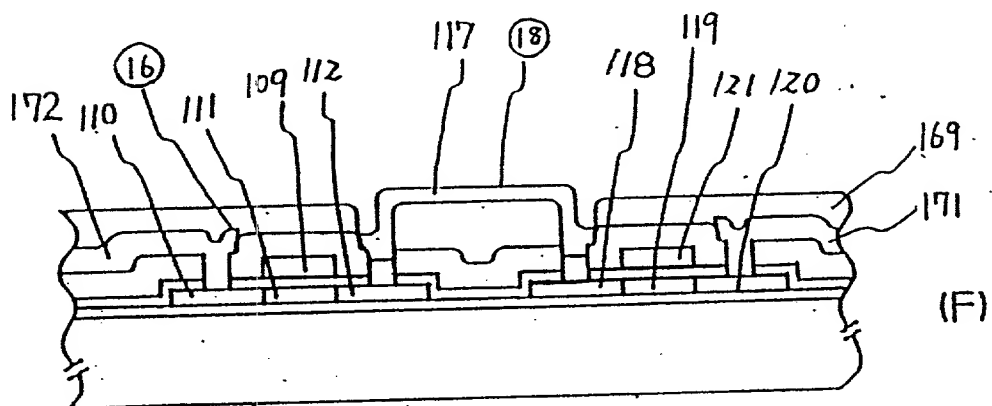
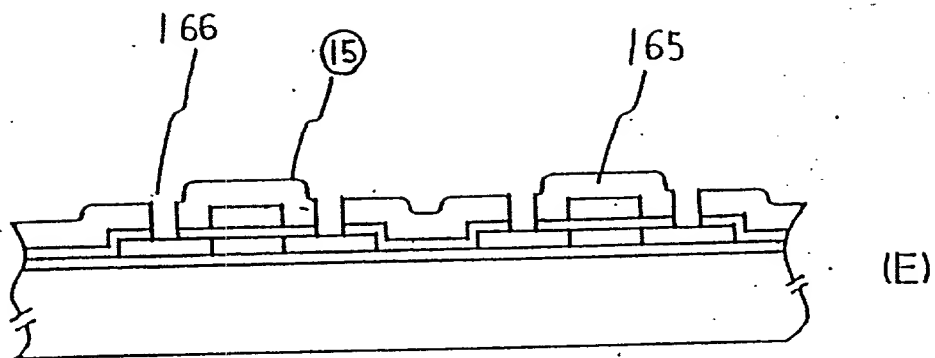
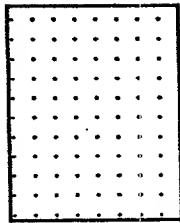
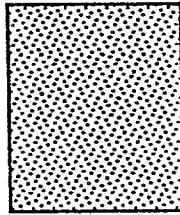


Fig. 14

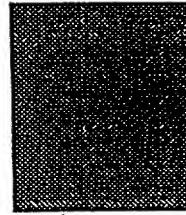
PIXEL A



PIXEL E



PIXEL C



# Fig. 15

$t / 16$   
 $\leftrightarrow^{227}$   $\xrightarrow{225}$

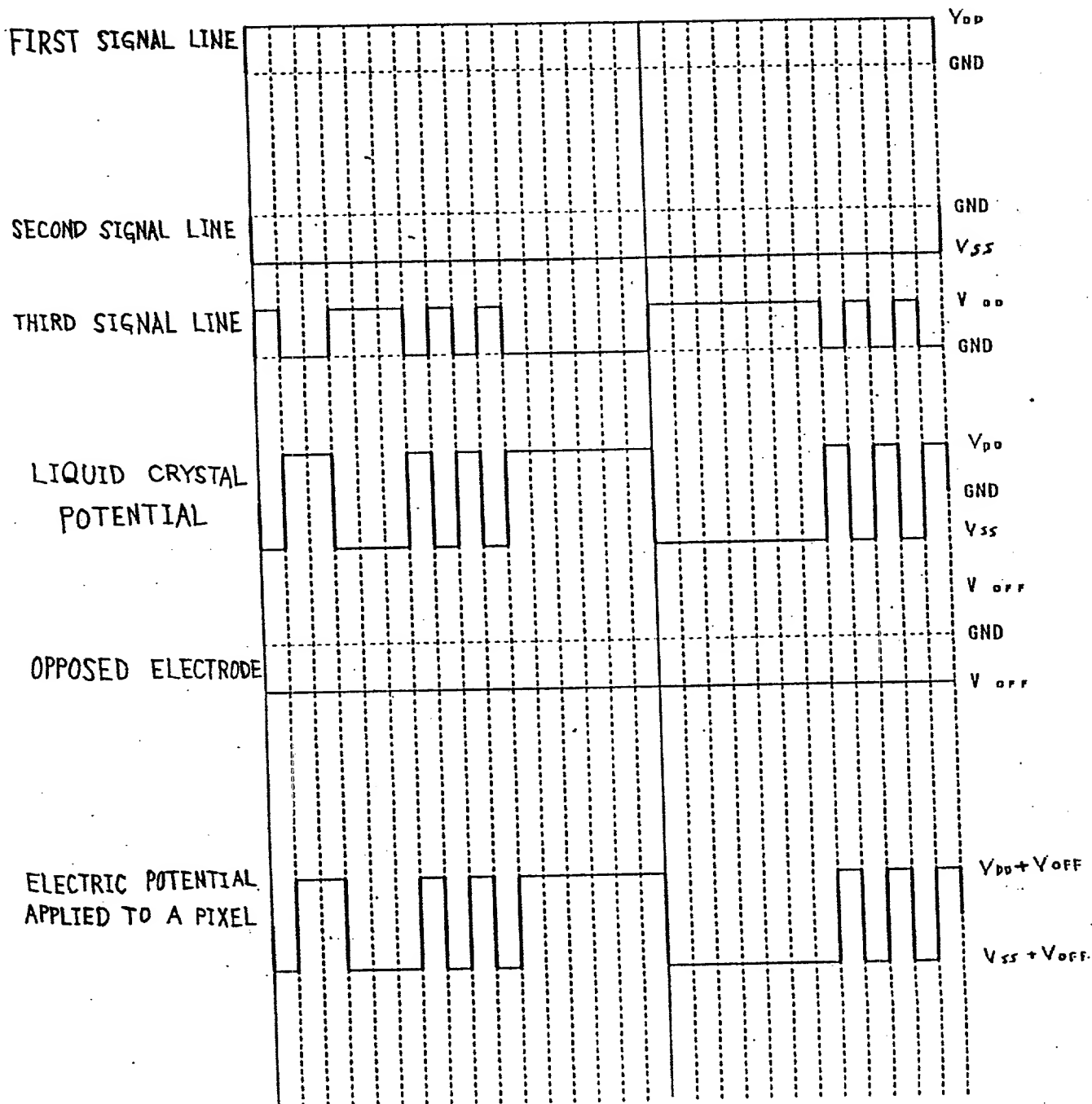




Fig. 16

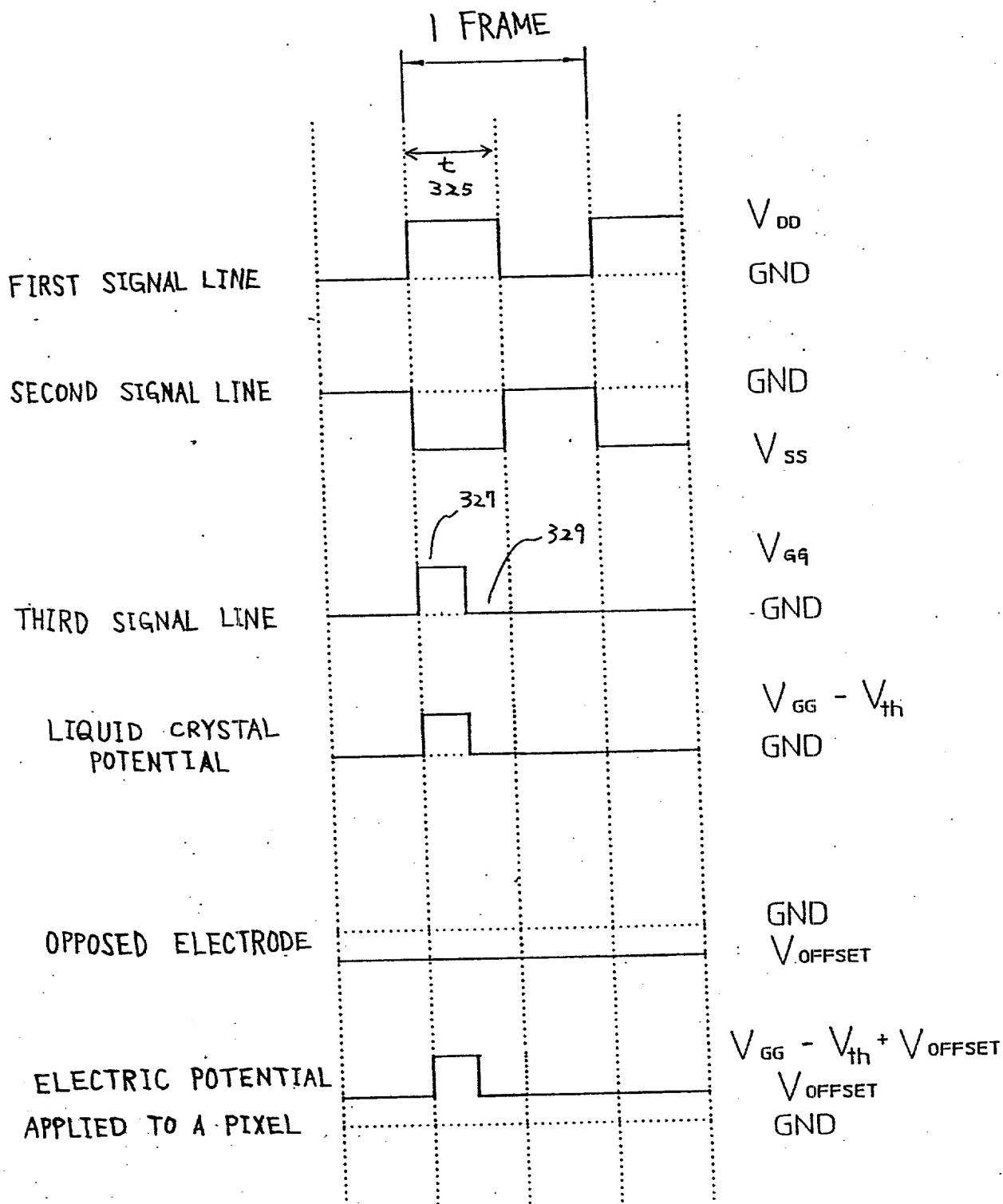


Fig. 17

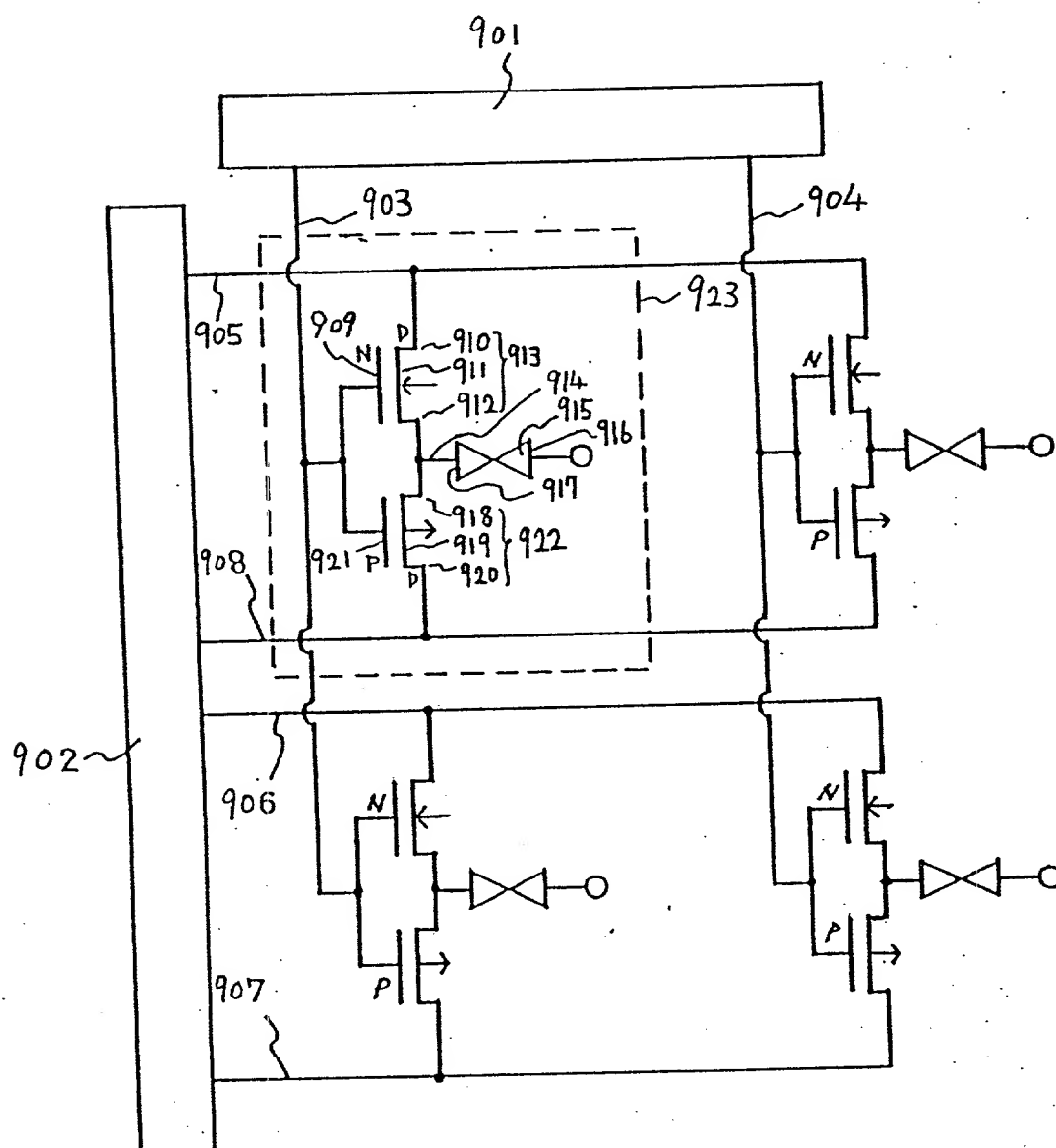


Fig. 18

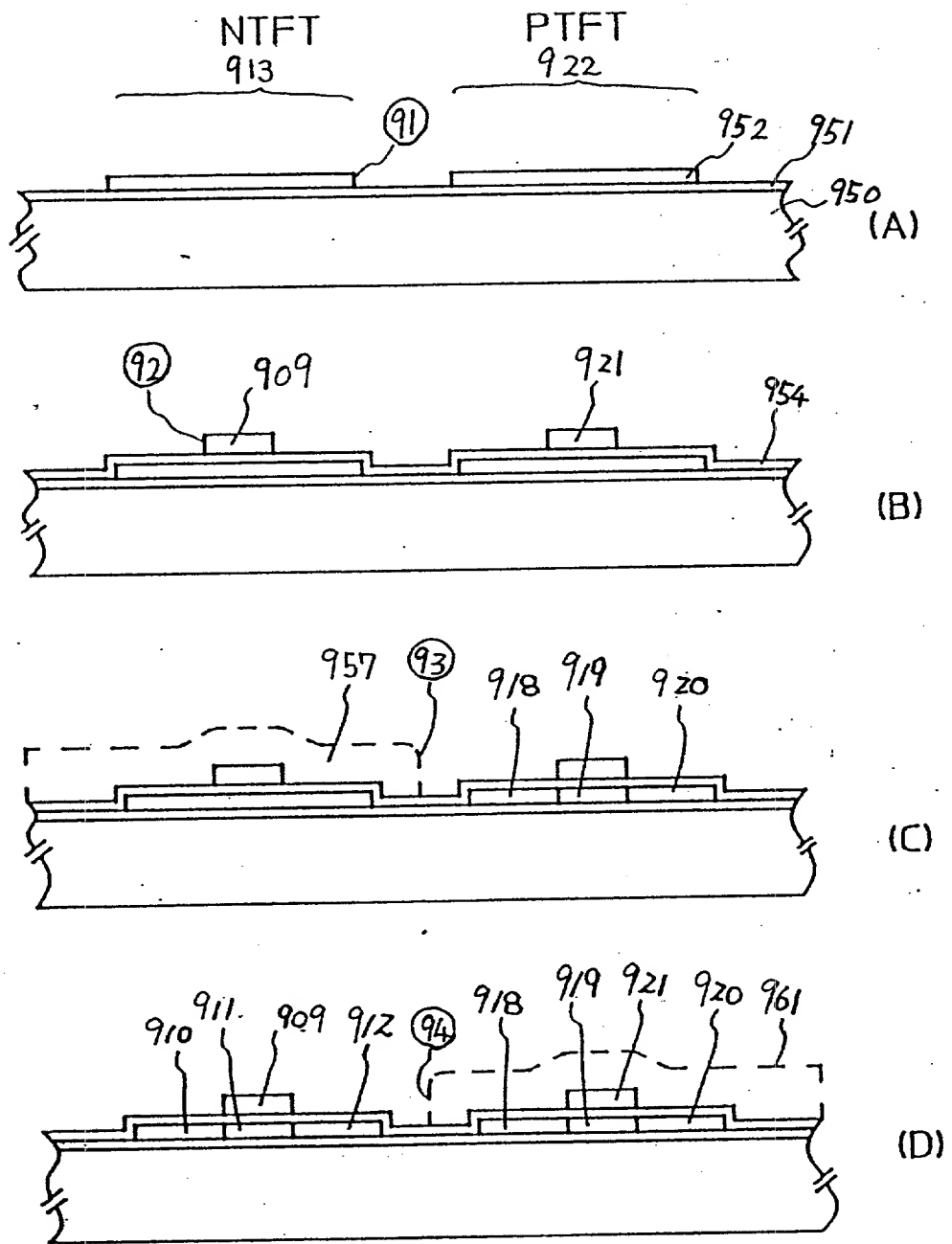


Fig. 18

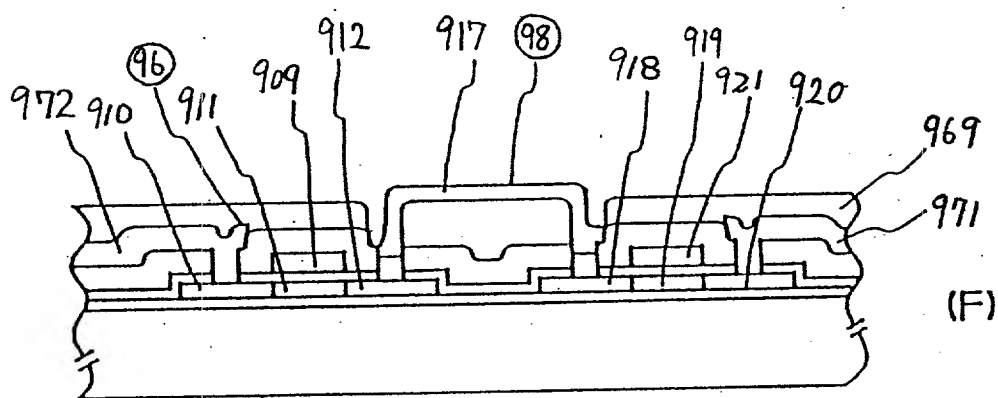
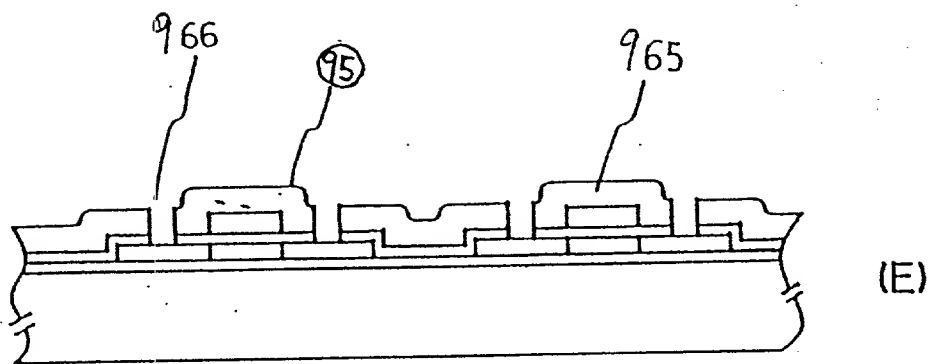


Fig. 19

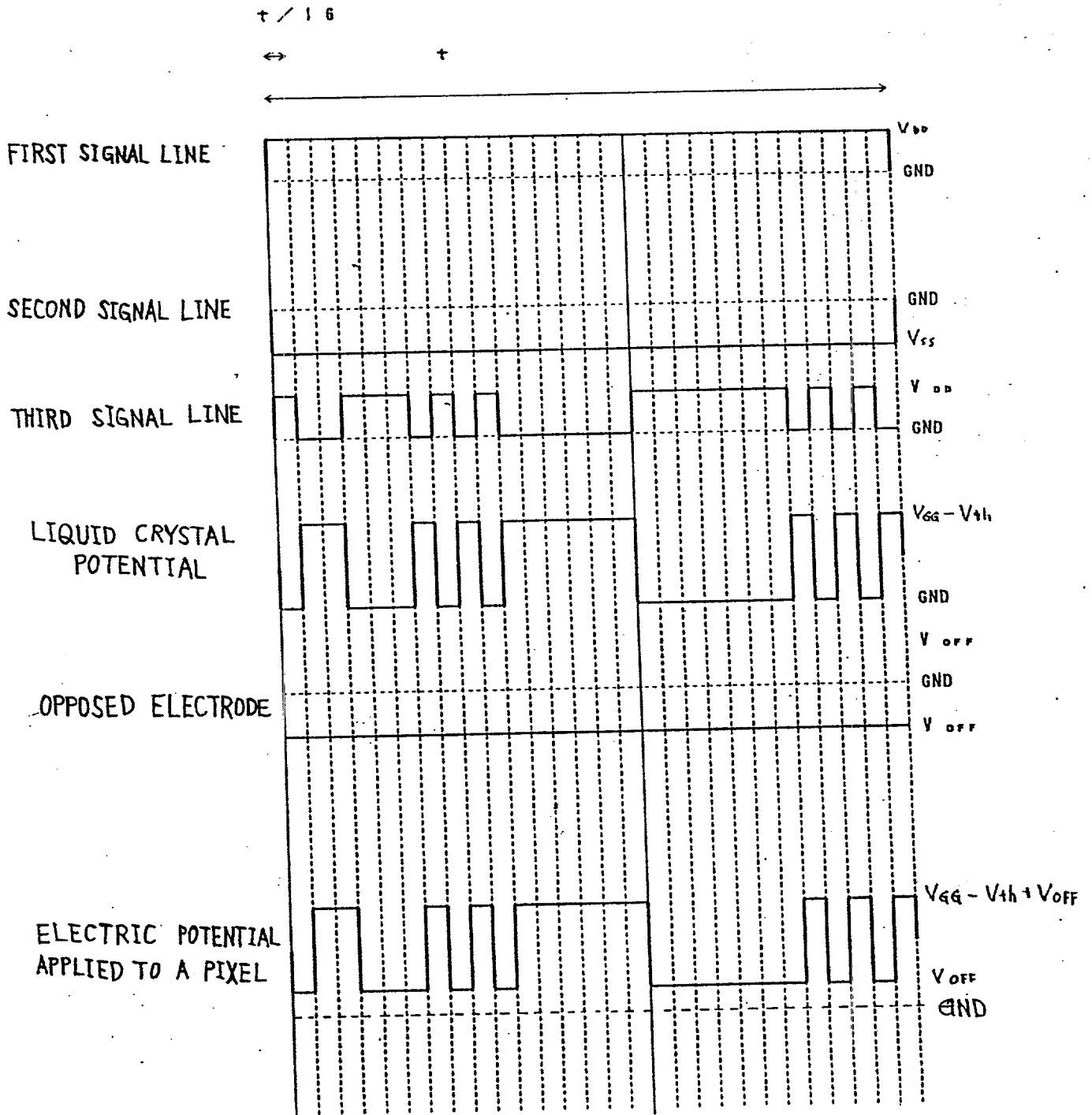


Fig. 20

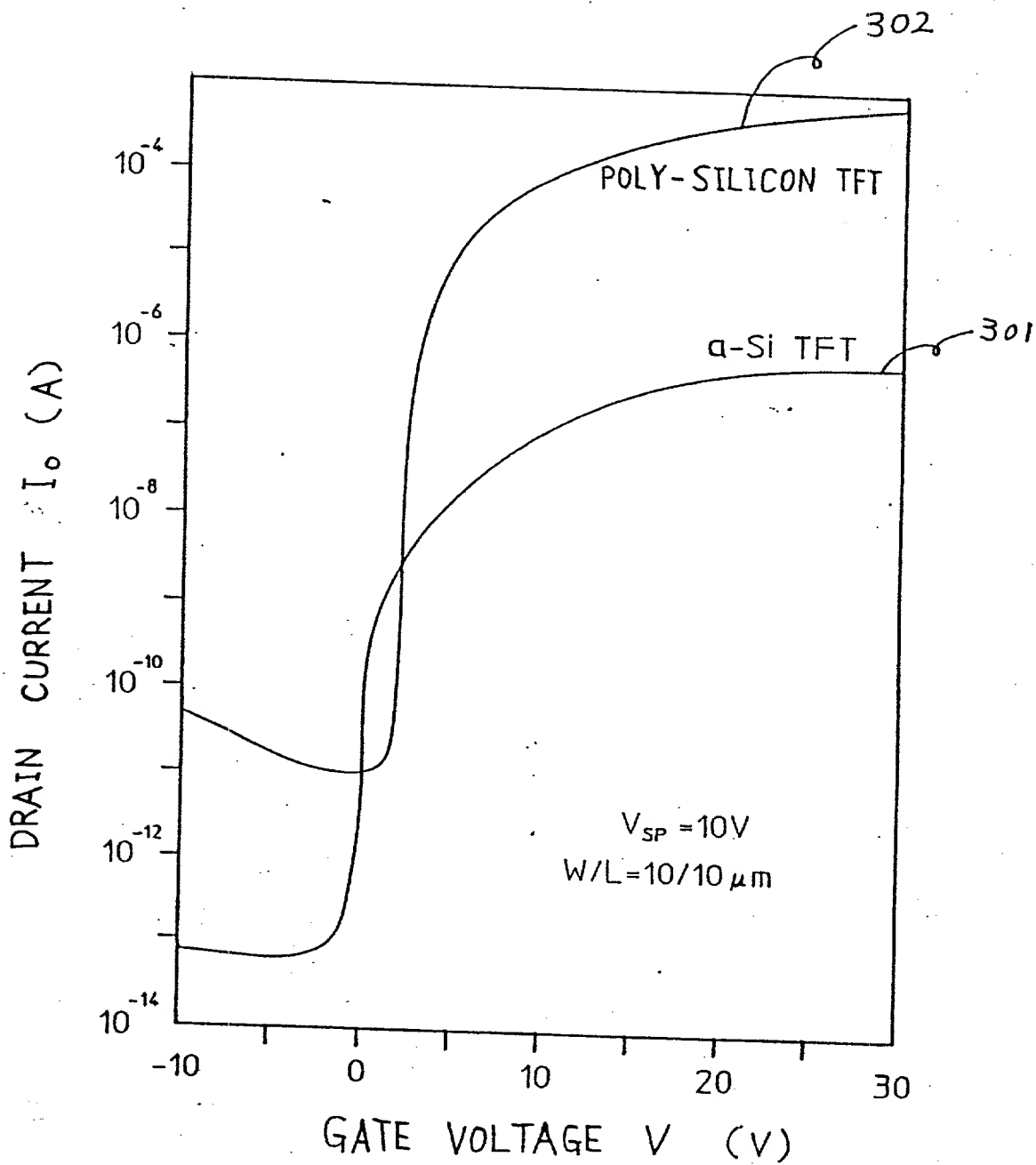


Fig. 21

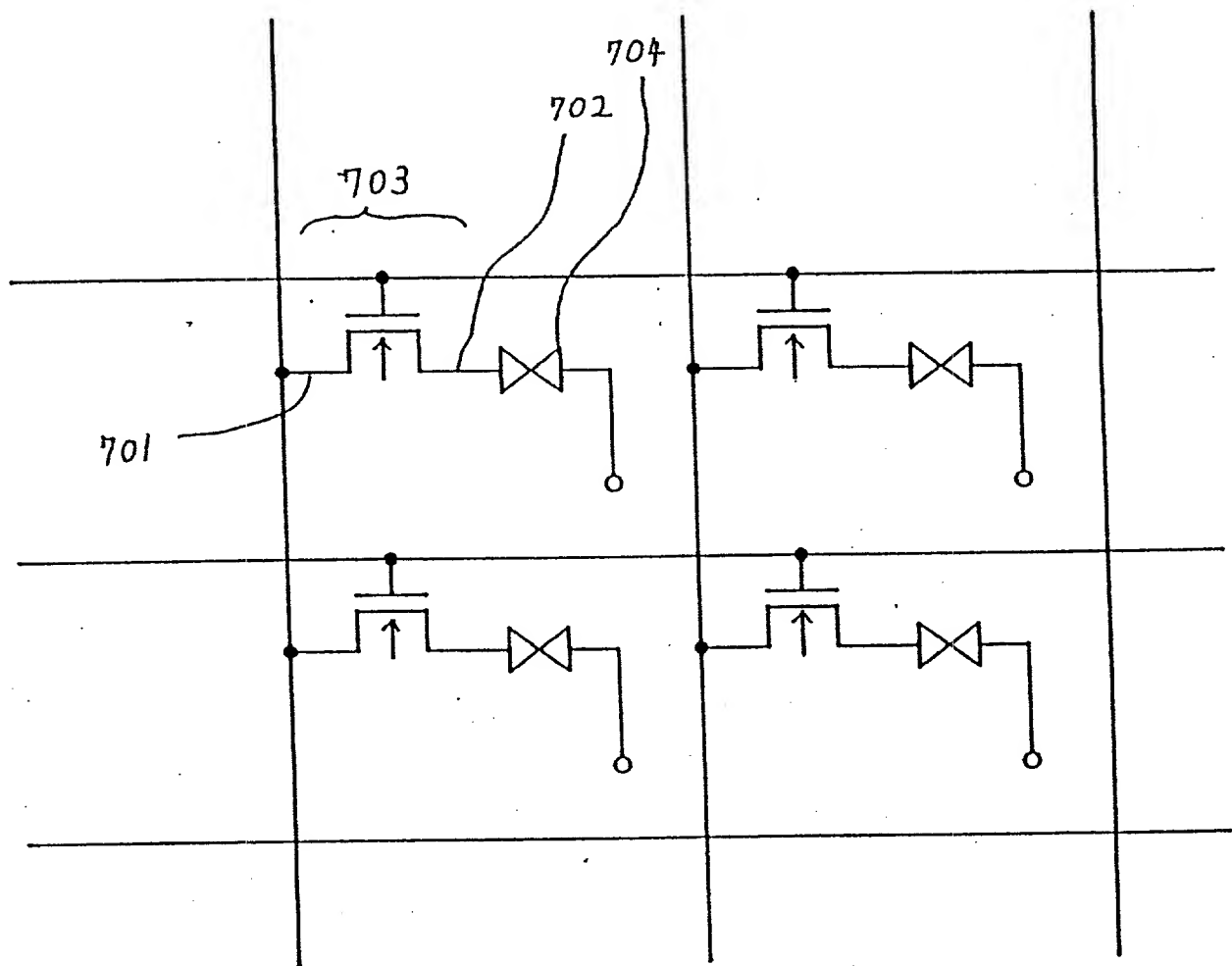


Fig. 22

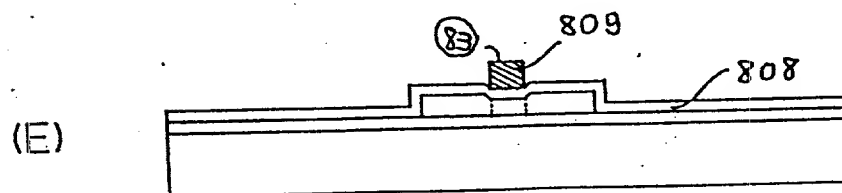
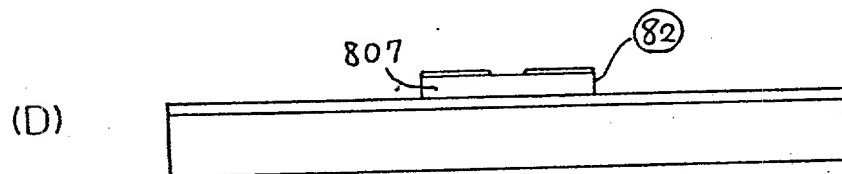
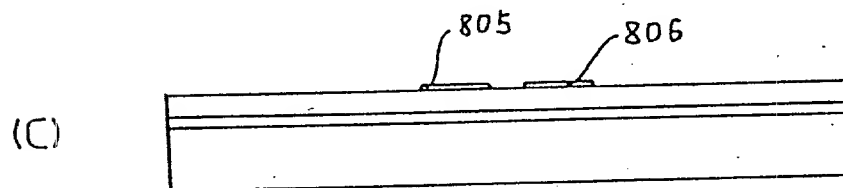
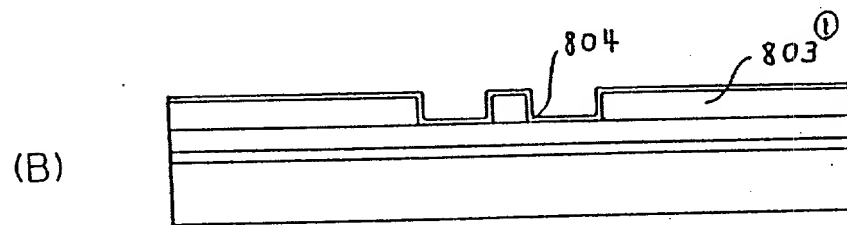
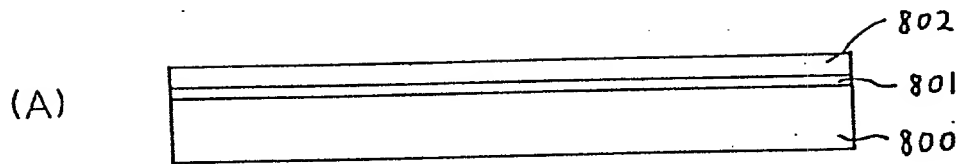




Fig. 22

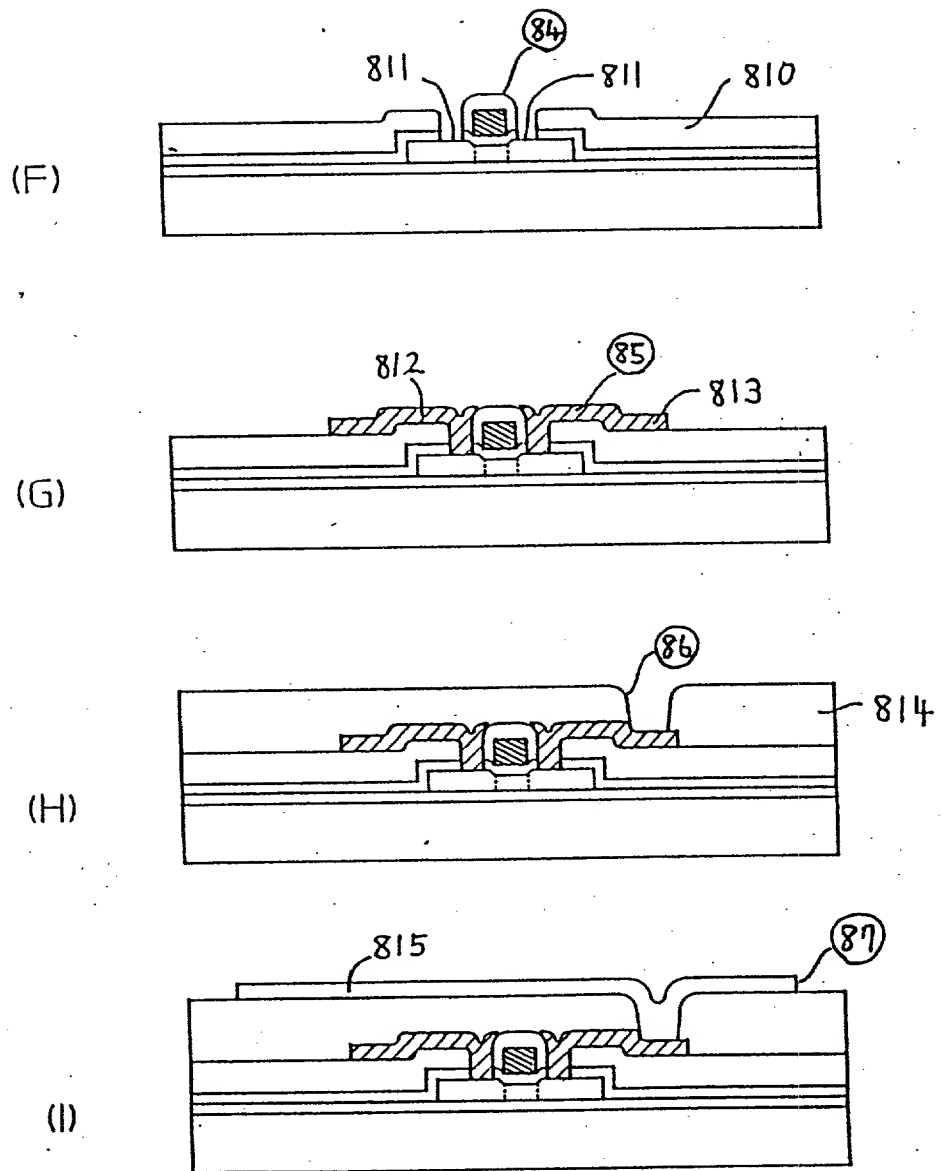


Fig. 23

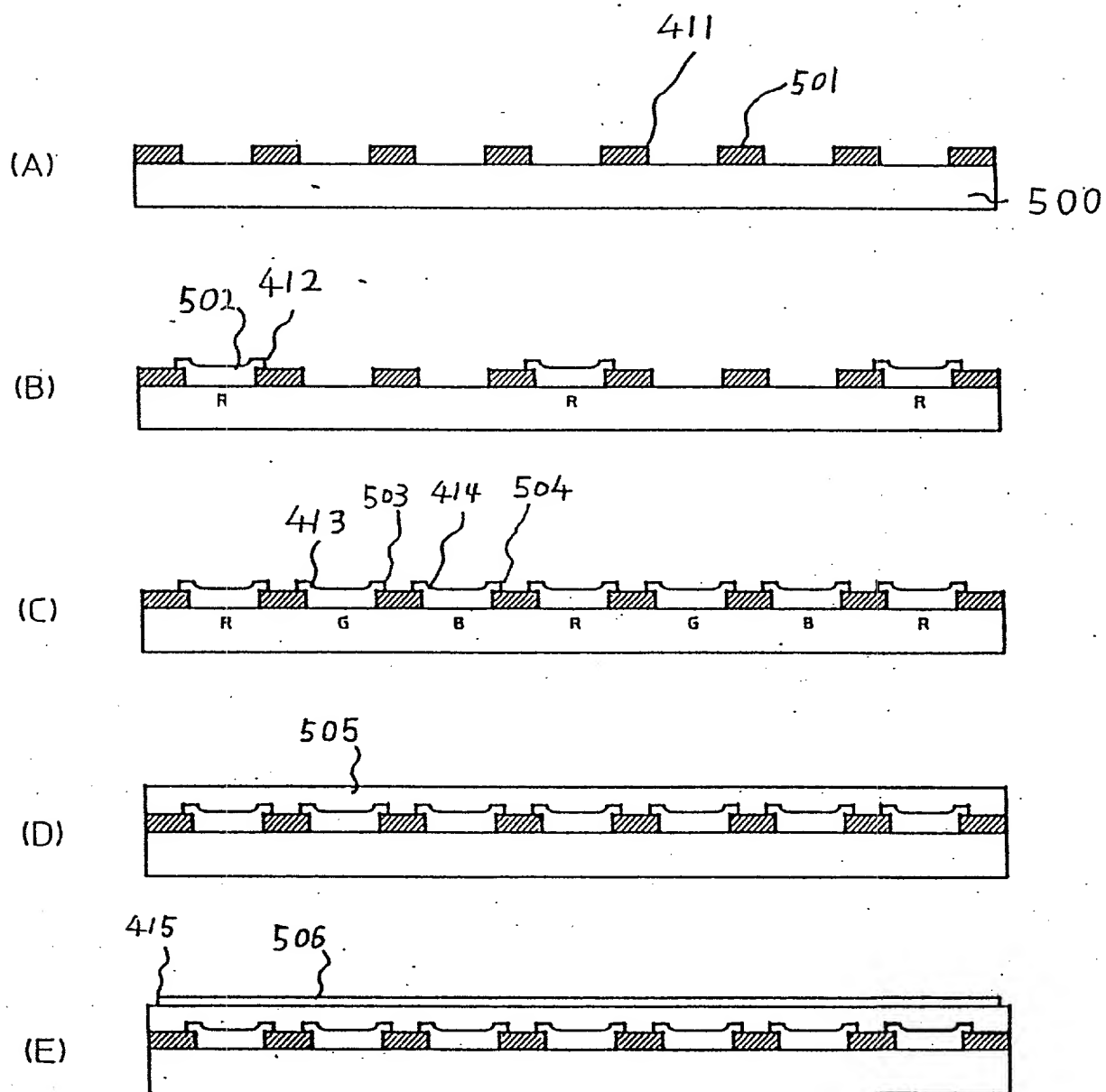


Fig. 24

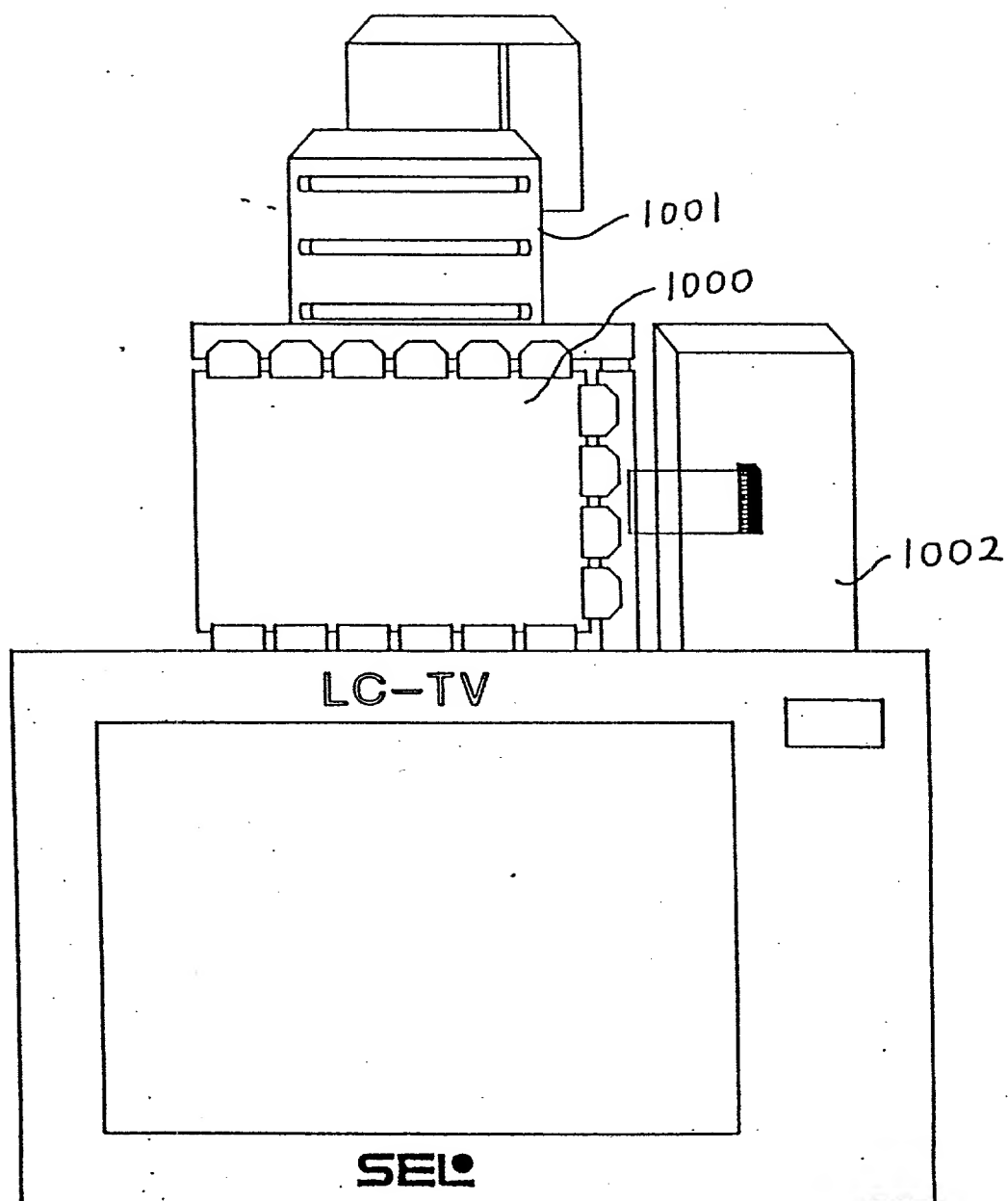


Fig. 25

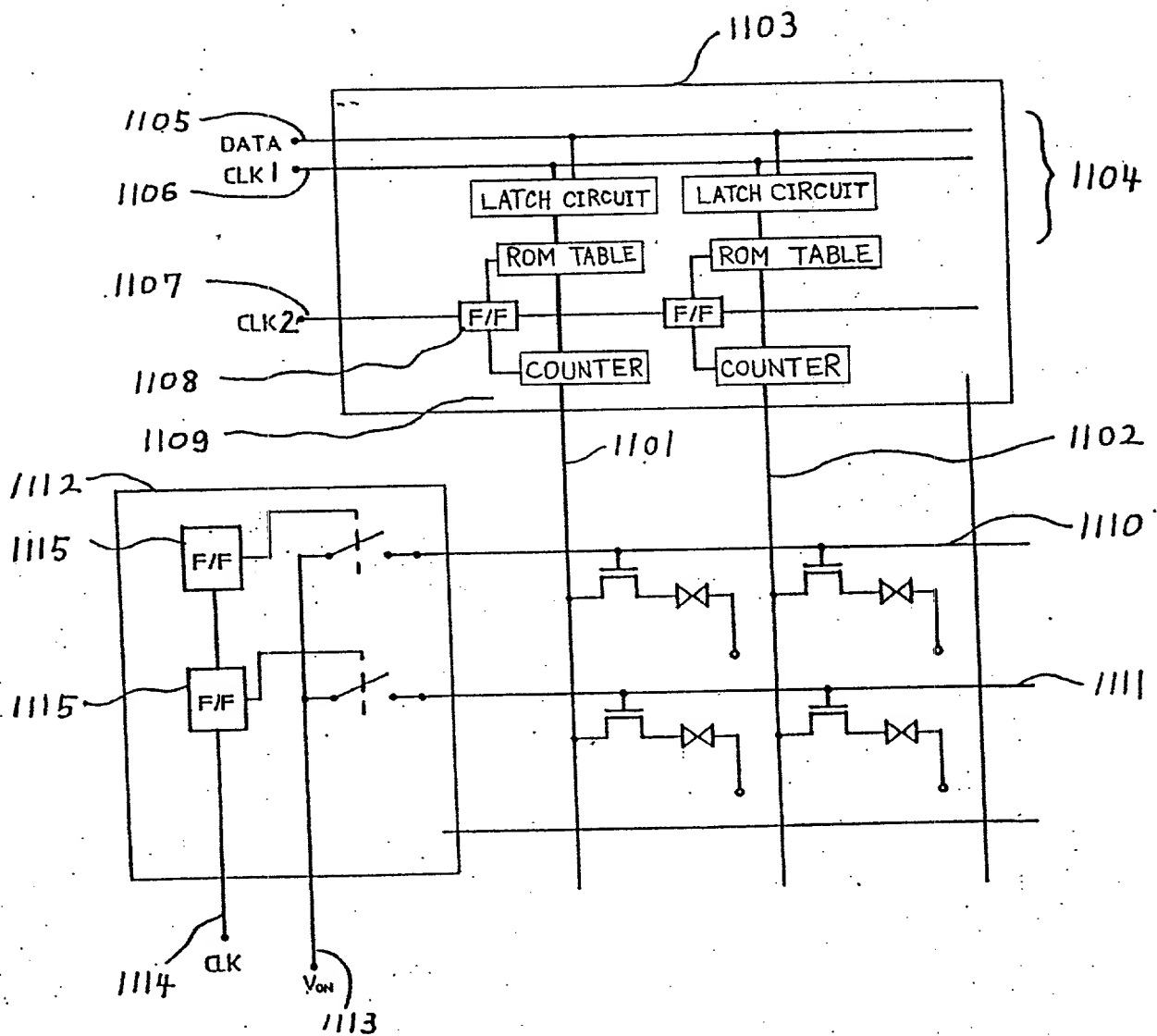


Fig. 26

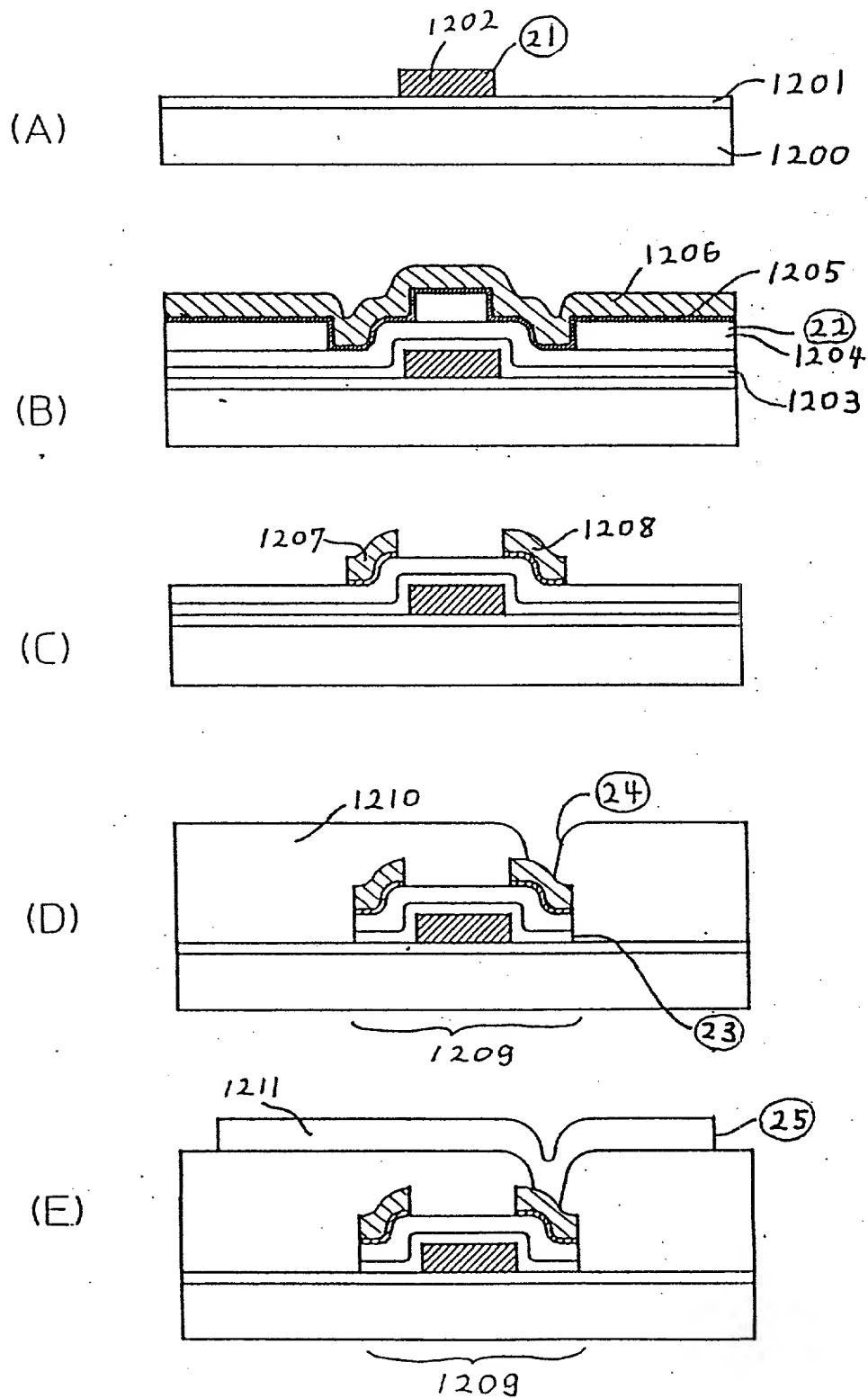


Fig. 27

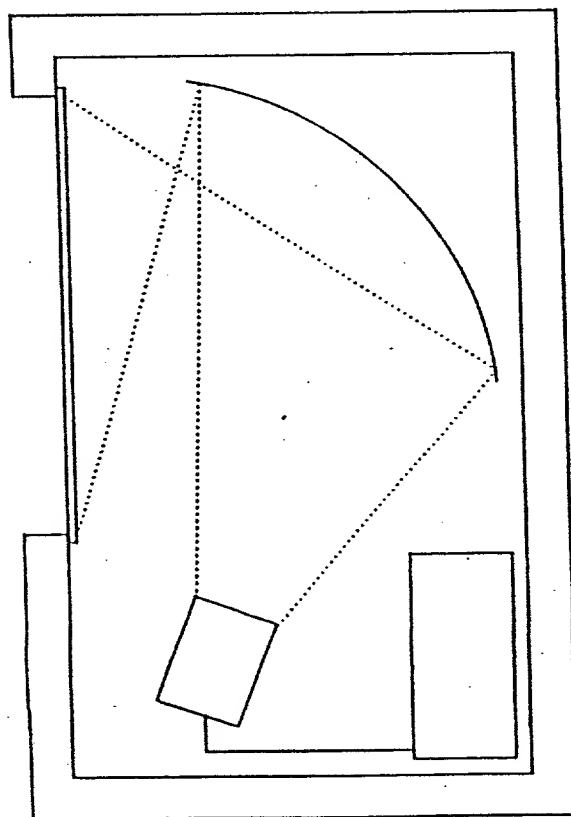
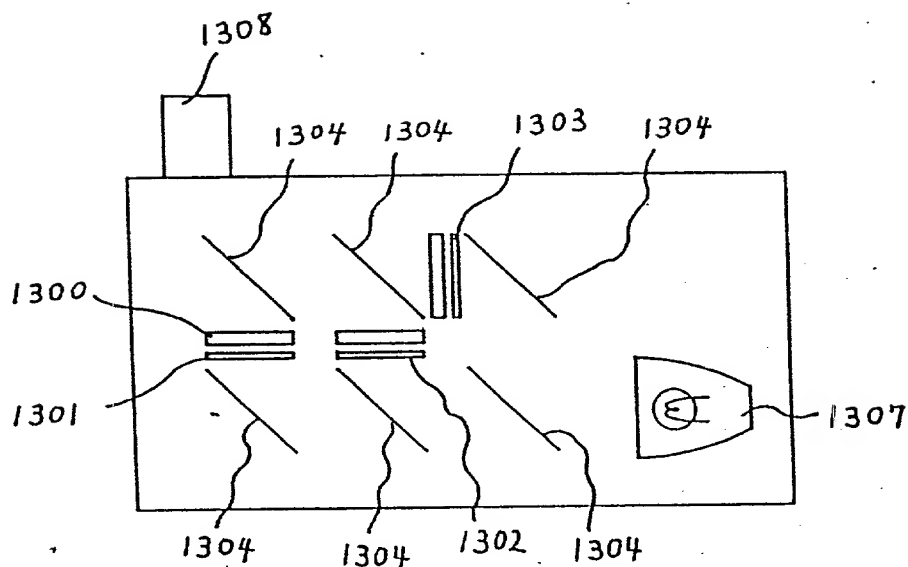


Fig. 28

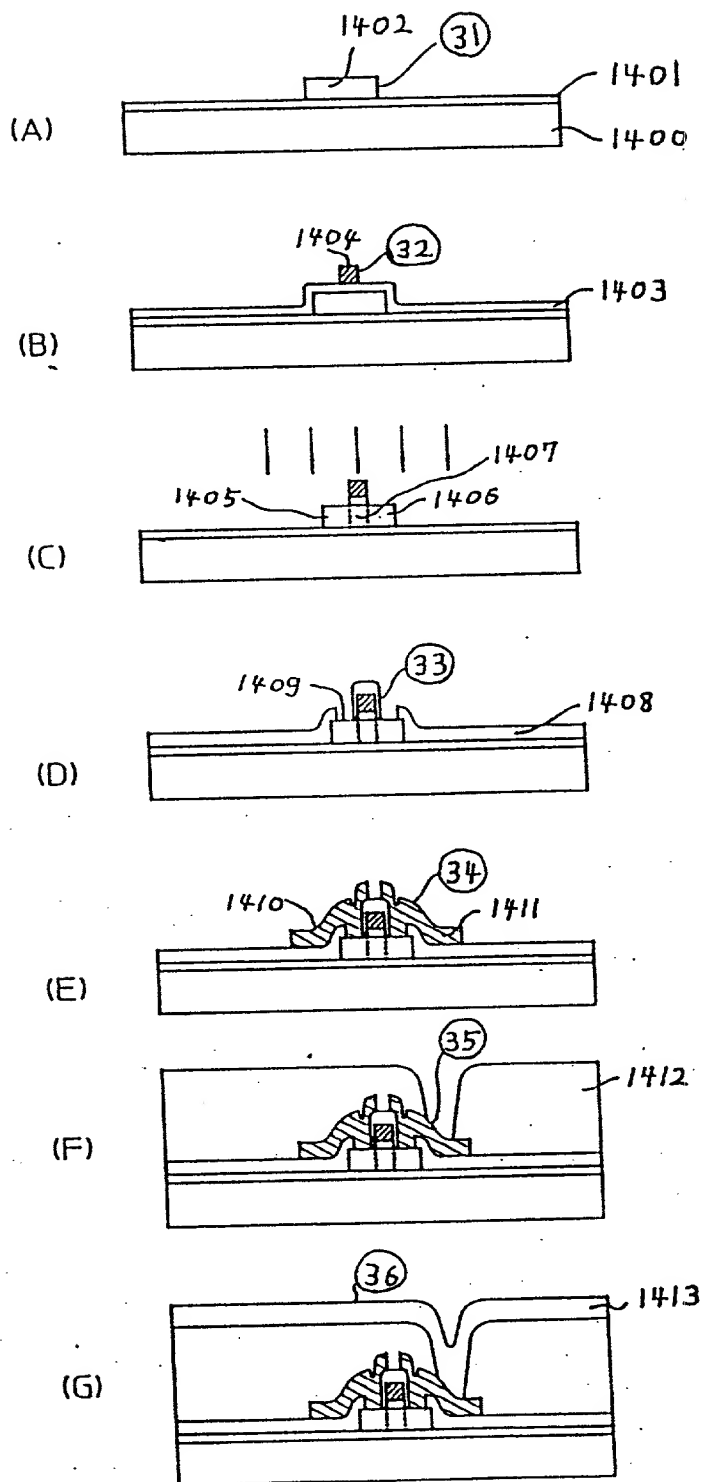
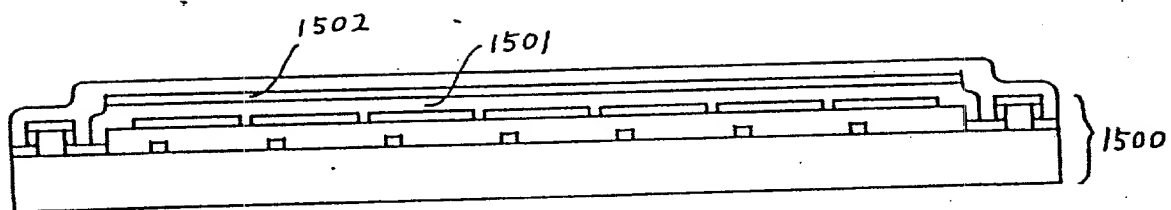


Fig. 29





	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415	2416	2417	2418	2419	2420	2421	2422	2
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Fig. 31

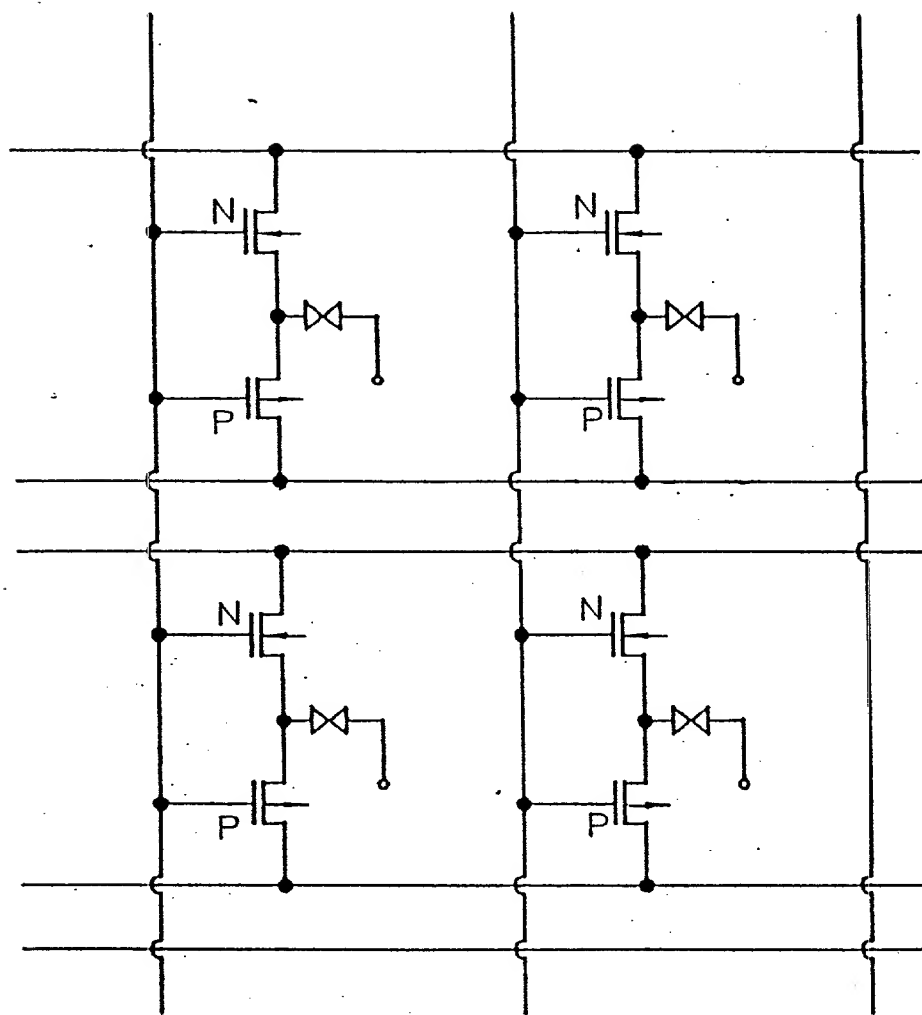


Fig. 32

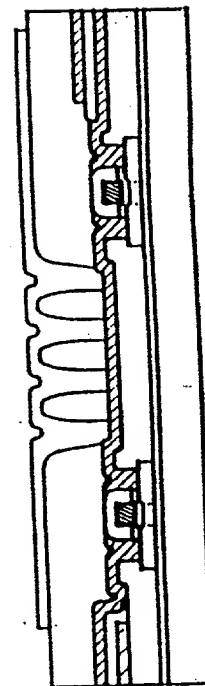
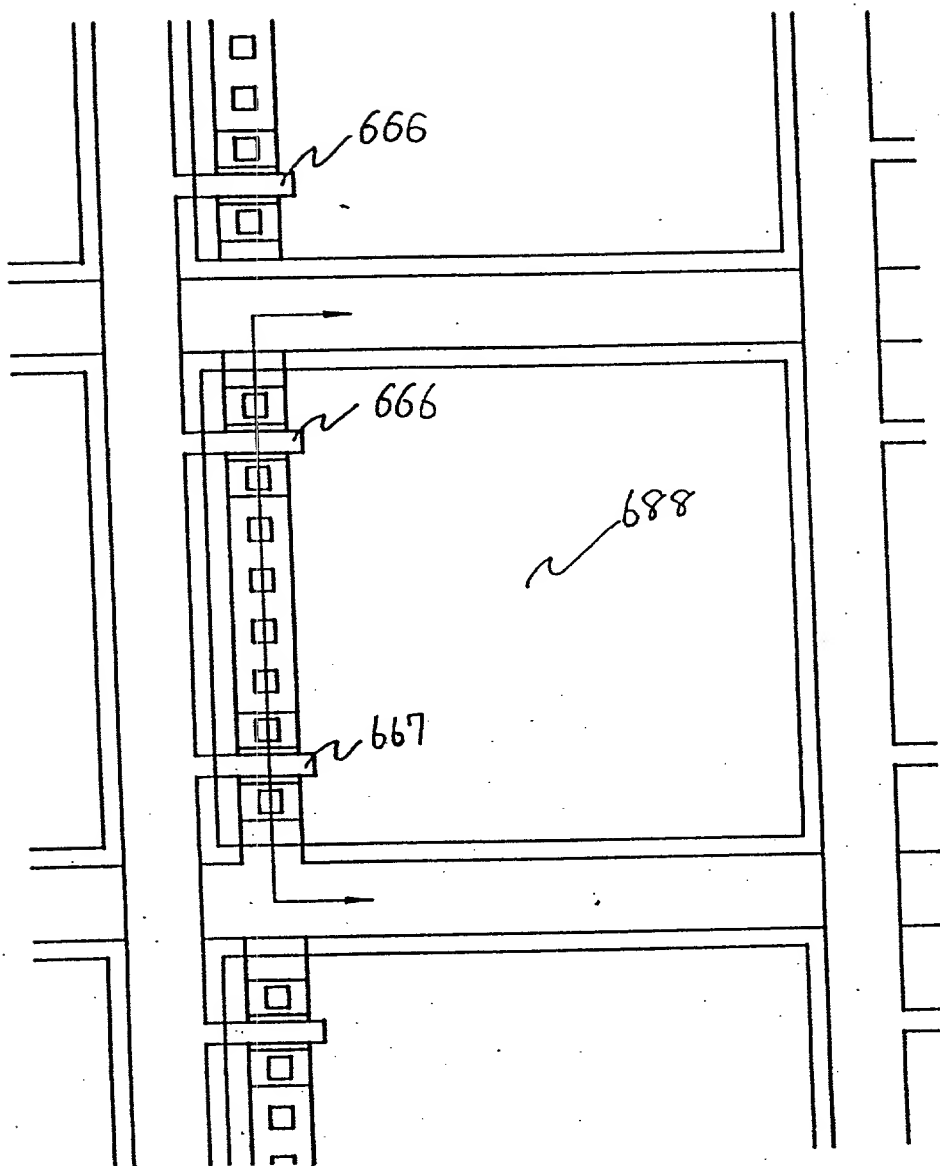


Fig. 33

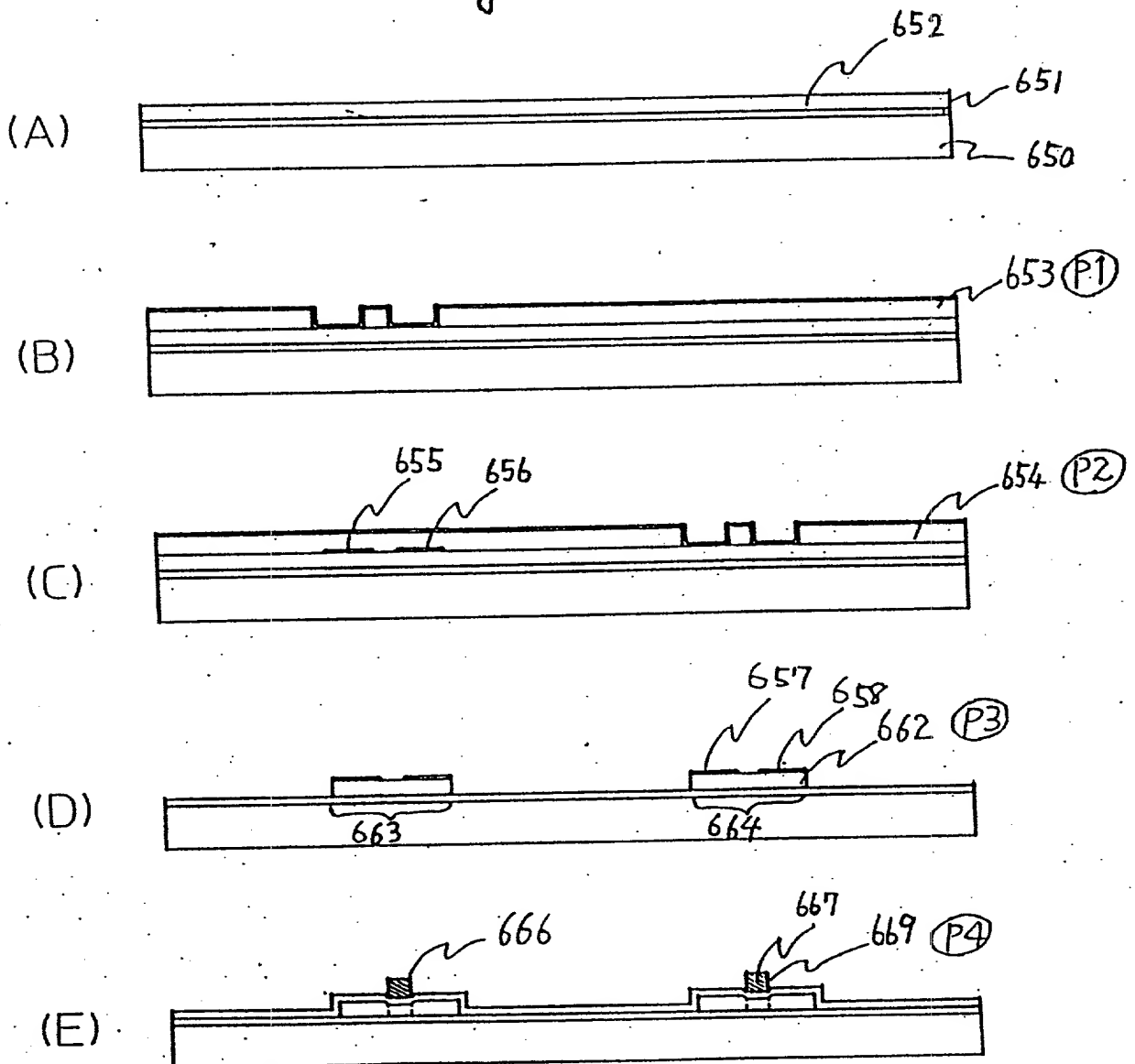
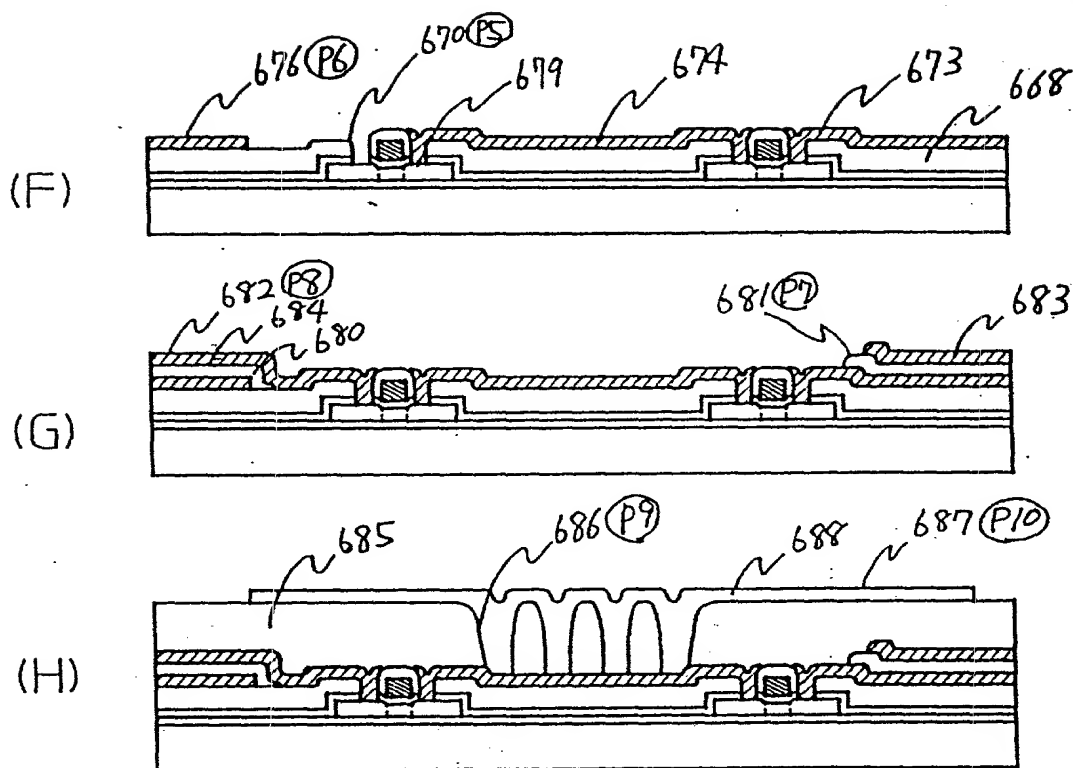


Fig. 33



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Fig. 34

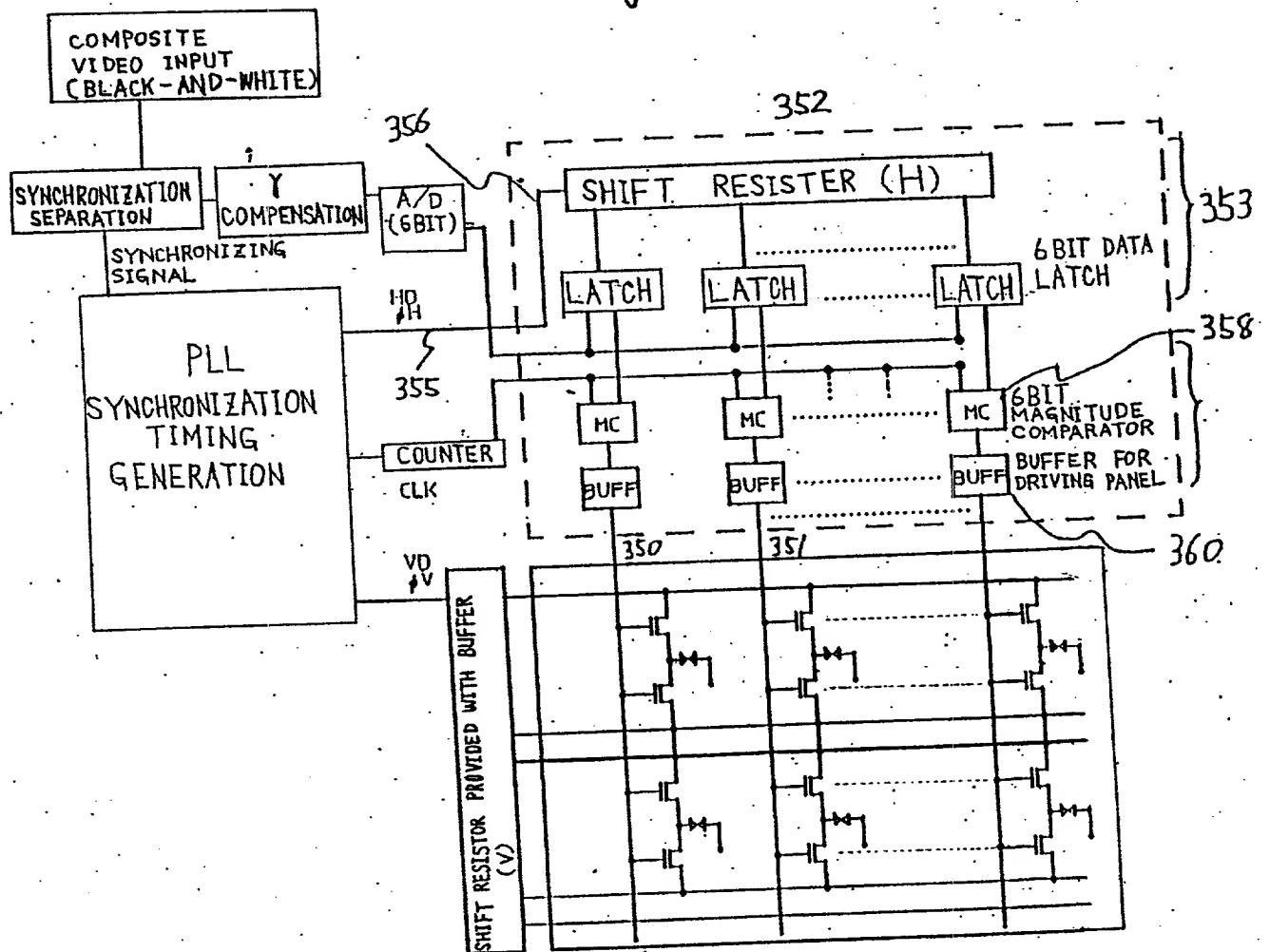
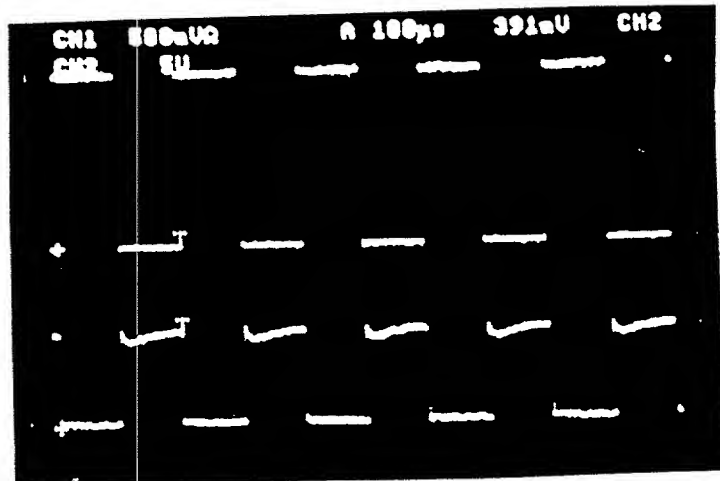


Fig. 35 (A)

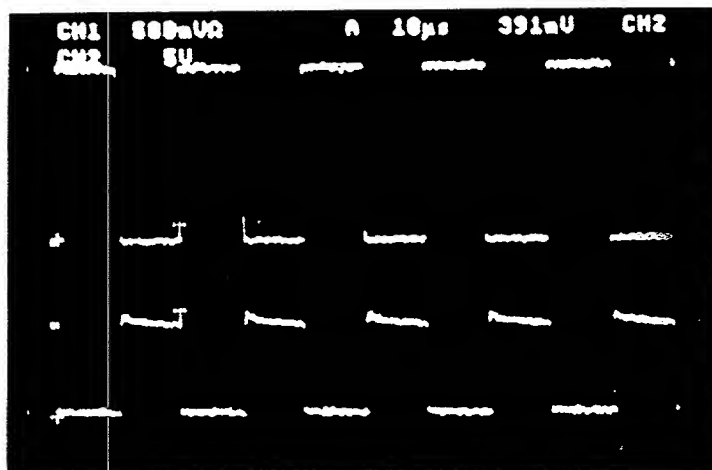
$f = 5 \text{ kHz}$



15V  
INPUT  
0V  
15V  
OUTPUT  
0V

Fig. 35 (B)

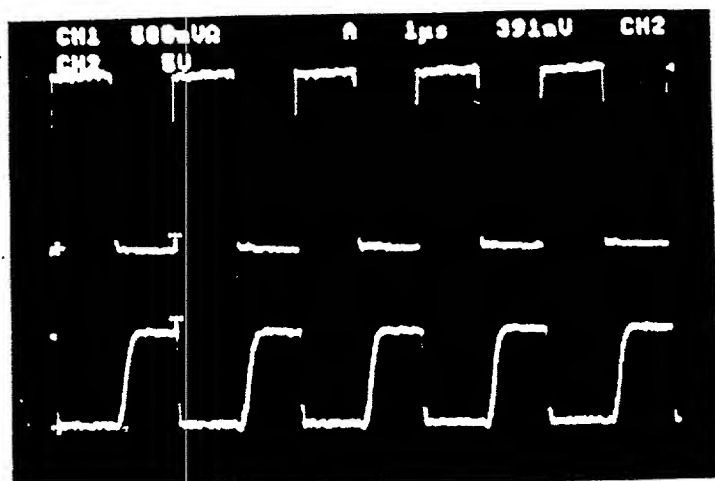
$f = 50 \text{ kHz}$



15V  
INPUT  
0V  
15V  
OUTPUT  
0V

Fig. 35 (C)

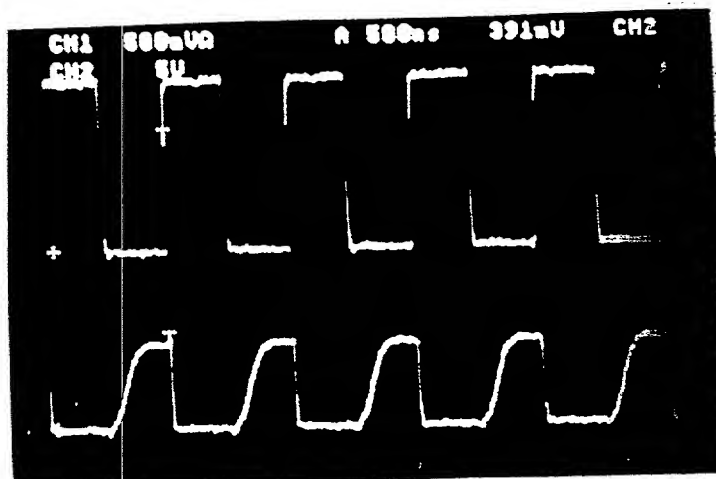
$$f = 500 \text{ kHz}$$



15V  
INPUT  
0V  
15V  
OUTPUT  
0V

Fig. 35 (D)

$$f = 1 \text{ MHz}$$

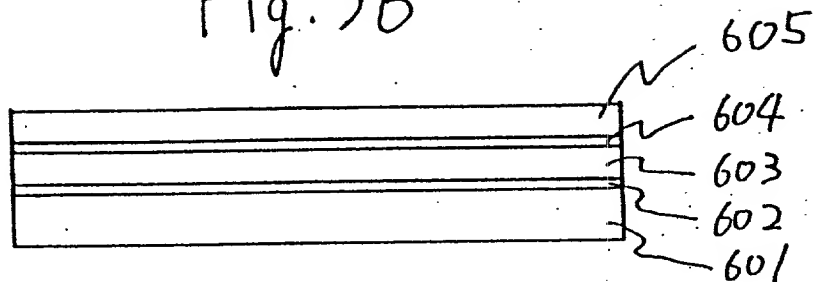


15V  
INPUT  
0V  
15V  
OUTPUT  
0V

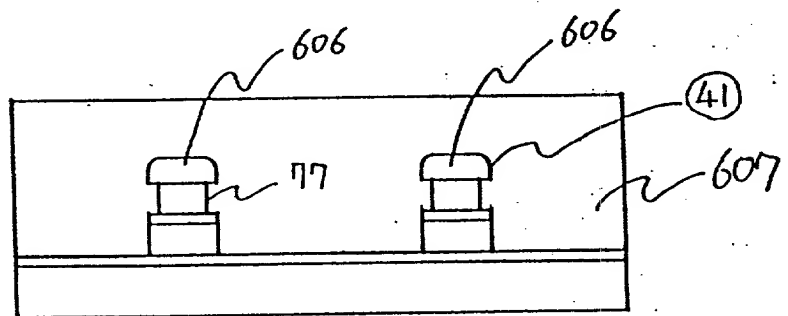


Fig. 36

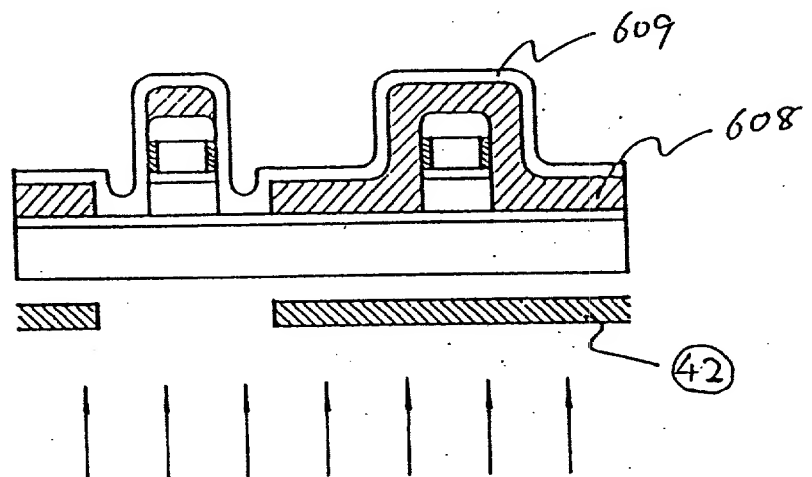
(A)



(B)



(C)



(D)

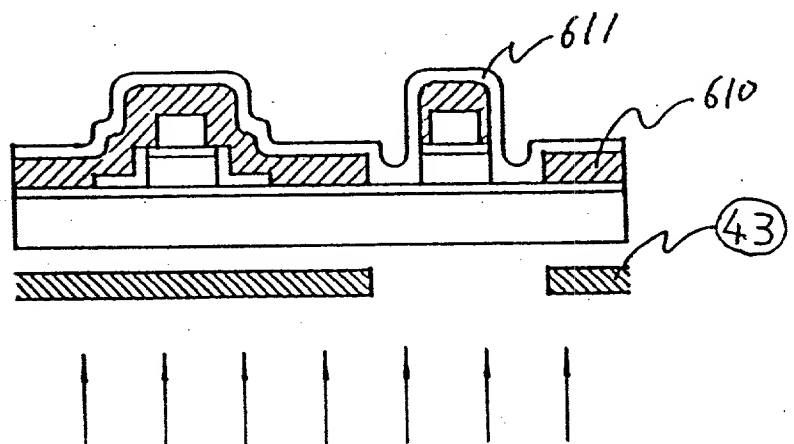
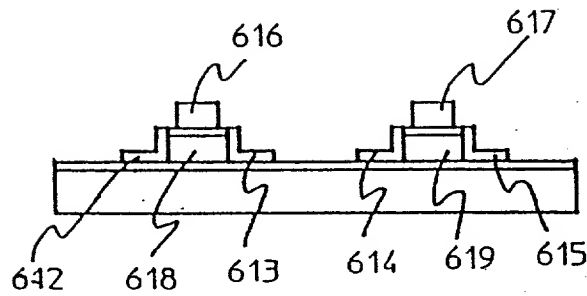
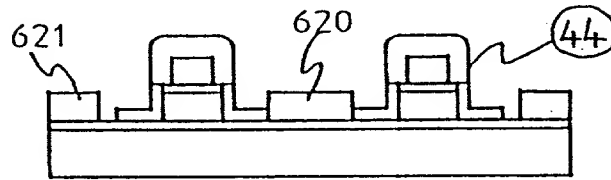


Fig. 36

(E)



(F)



(G)

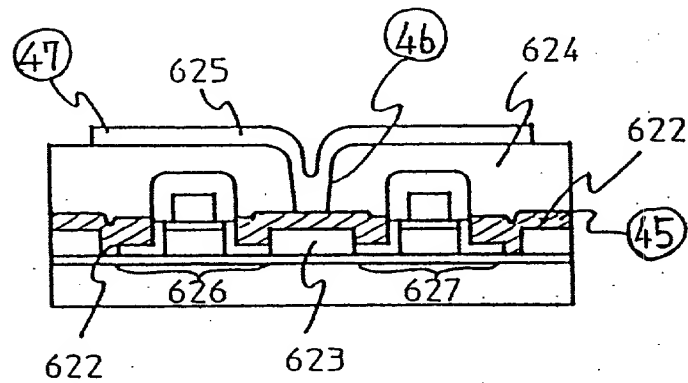


Fig. 37

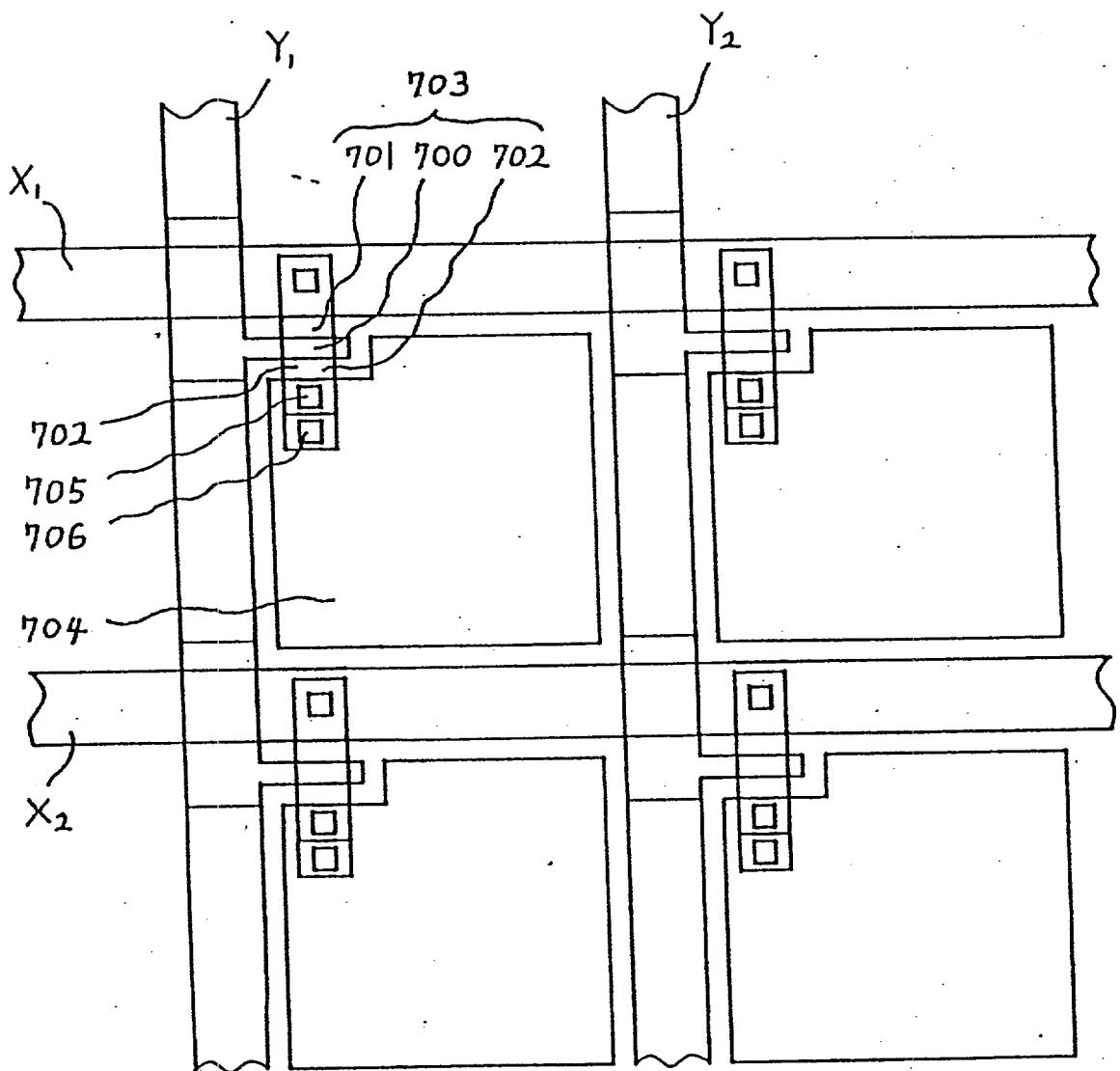


Fig. 38

